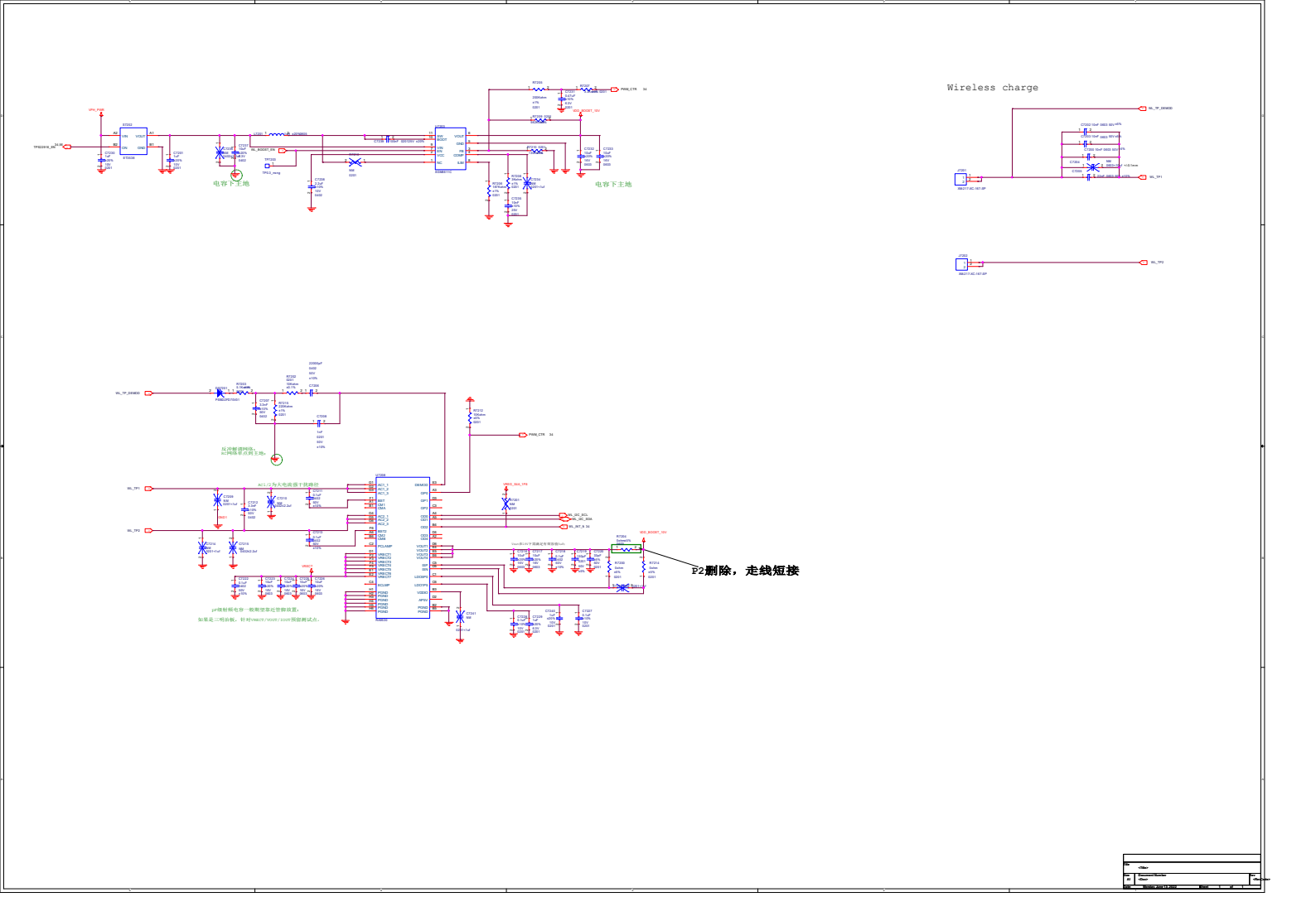
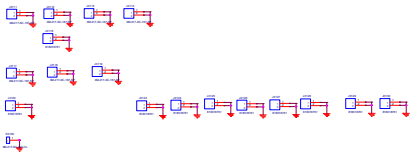

Wireless charge
电容下主地
电容下主地
反冲耦合网络，
AC网络单点到主地。
AC1/2为大电流低下线路
P2删除，走线短接

GND



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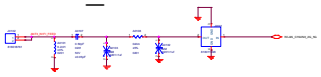
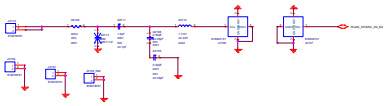
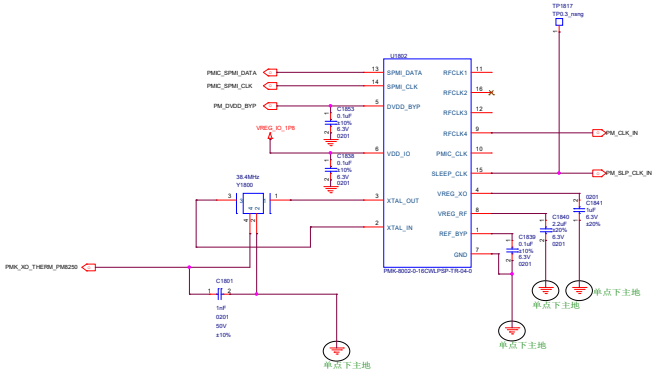


WIFI_CH1



Place XO as close to PMK8002 as possible, away from heat source in all directions (including Z-direction for stacked PCB).
Route XTAL_IN and XTAL_OUT traces on surface layer only with length <18mm
No trace shall be powered in at least two immediate layers below XTAL.
Refer to 80-VP447-10 for XO Layout App Note



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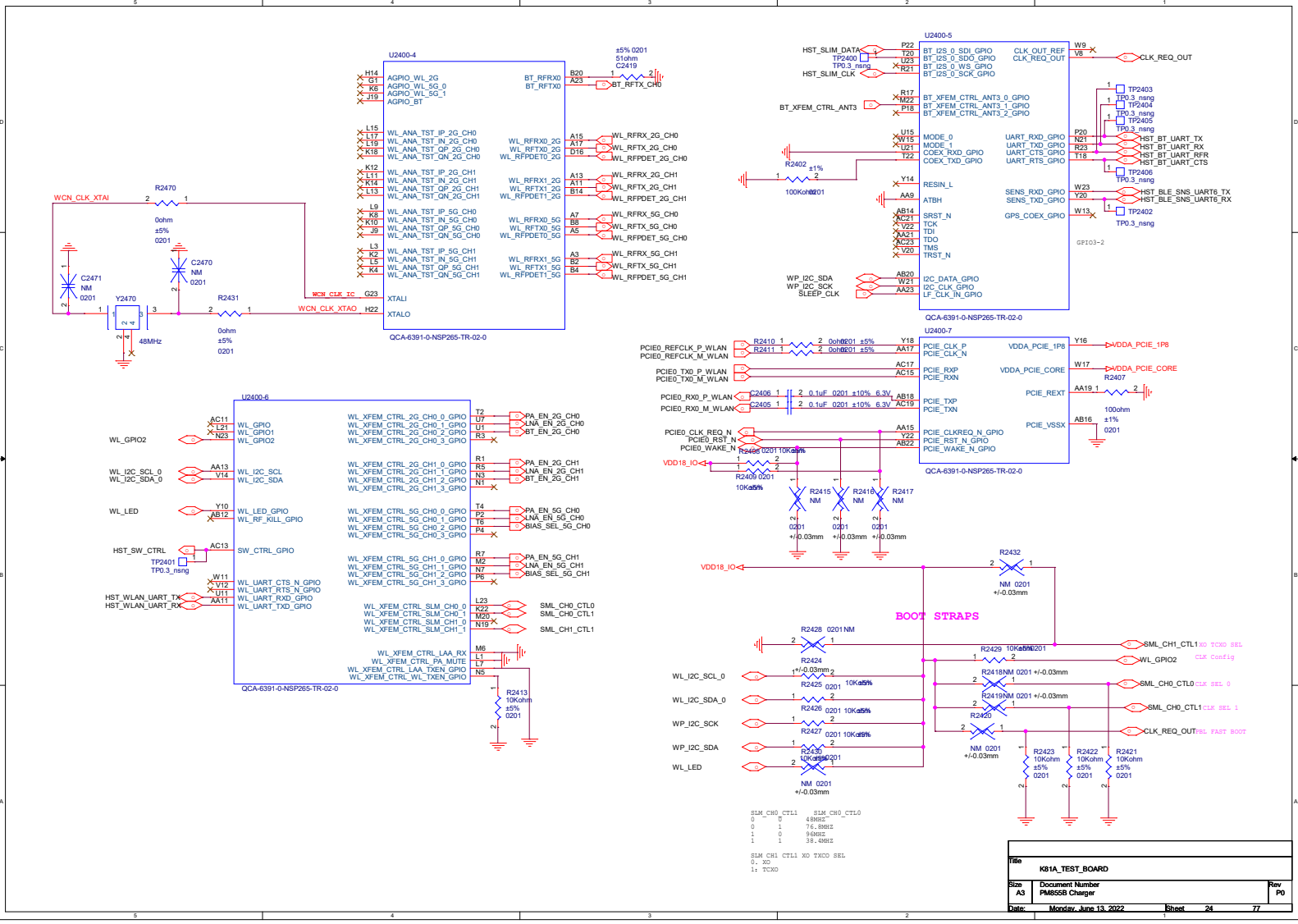
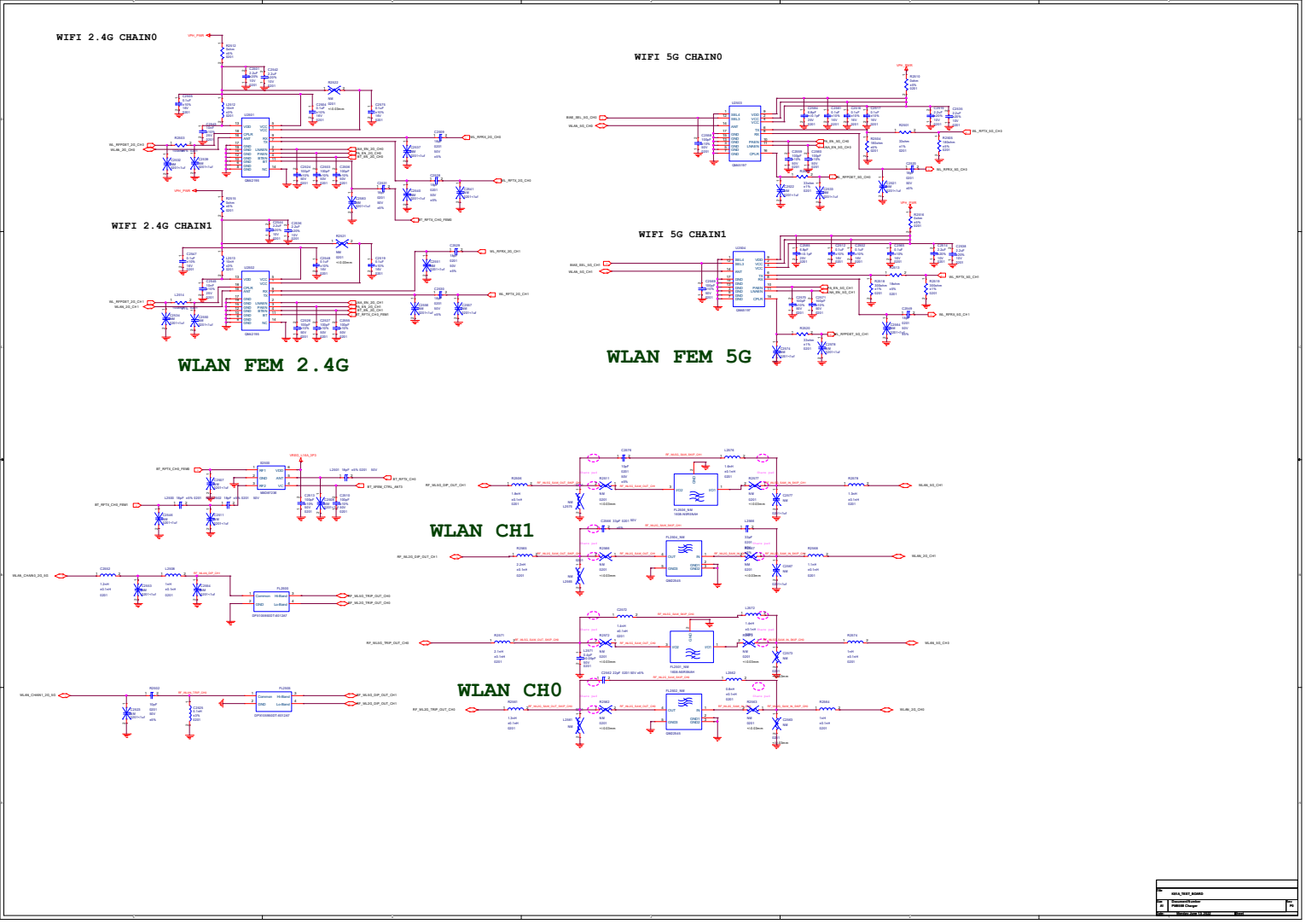
Size: A2	Document Number: Reserved(for SG-WTR I) — Rev: P0
Date: Monday, June 13, 2022	Sheet


U2400-4
QCA-6391-0-NSP265-TR-02-0
U2400-5
QCA-6391-0-NSP265-TR-02-0
U2400-7
QCA-6391-0-NSP265-TR-02-0
U2400-6
QCA-6391-0-NSP265-TR-02-0
WCN_CLK_XTAI
WCN_CLK_XTAO
R2470
0ohm
±5%
0201
C2471
NM
0201
C2470
NM
0201
Y2470
48MHz
R2431
0ohm
±5%
0201
±5% 0201
51ohm
C2419
BT_RFTX_CH0
WL_RFRX_2G_CH0
WL_RFTX_2G_CH0
WL_RFPDET_2G_CH0
WL_RFRX_2G_CH1
WL_RFTX_2G_CH1
WL_RFPDET_2G_CH1
WL_RFRX_5G_CH0
WL_RFTX_5G_CH0
WL_RFPDET_5G_CH0
WL_RFRX_5G_CH1
WL_RFTX_5G_CH1
WL_RFPDET_5G_CH1
HST_SLIM_DATA
HST_SLIM_CLK
BT_XFEM_CTRL_ANT3
CLK_REQ_OUT
HST_BT_UART_TX
HST_BT_UART_RX
HST_BT_UART_RFR
HST_BT_UART_CTS
HST_BLE_SNS_UART6_TX
HST_BLE_SNS_UART6_RX
WP_I2C_SDA
WP_I2C_SCK
SLEEP_CLK
R2402
100Kohm
PCIE0_REFCLK_P_WLAN
PCIE0_REFCLK_M_WLAN
PCIE0_TX0_P_WLAN
PCIE0_TX0_M_WLAN
PCIE0_RX0_P_WLAN
PCIE0_RX0_M_WLAN
PCIE0_CLK_REQ_N
PCIE0_RST_N
PCIE0_WAKE_N
VDD18_IO
VDDA_PCIE_1P8
VDDA_PCIE_CORE
R2407
100ohm
±1%
0201
R2415
R2418
R2417
NM
+/-0.03mm
R2432
BOOT STRAPS
R2428
R2424
R2425
R2426
R2427
R2430
R2429
R2418
R2419
R2420
R2423
R2422
R2421
10Kohm
±5%
0201
WL_I2C_SCL_0
WL_I2C_SDA_0
WP_I2C_SCK
WP_I2C_SDA
WL_LED
SML_CH1_CTL1
WL_GPIO2
SML_CH0_CTL0
CLK_REQ_OUT
XO TCXO SEL
CLK Config
CLK SEL 0
CLK SEL 1
SEL FAST BOOT
WL_GPIO2
WL_I2C_SCL_0
WL_I2C_SDA_0
WL_LED
HST_SW_CTRL
HST_WLAN_UART_TX
HST_WLAN_UART_RX
PA_EN_2G_CH0
LNA_EN_2G_CH0
BT_EN_2G_CH0
PA_EN_2G_CH1
LNA_EN_2G_CH1
BT_EN_2G_CH1
PA_EN_5G_CH0
LNA_EN_5G_CH0
BIAS_SEL_5G_CH0
PA_EN_5G_CH1
LNA_EN_5G_CH1
BIAS_SEL_5G_CH1
SML_CH0_CTL0
SML_CH0_CTL1
SML_CH1_CTL1
R2413
10Kohm
±5%
0201
SLM_CH0_CTL1 SLM_CH0_CTL0
0 0 48MHZ
0 1 76.8MHZ
1 0 96MHZ
1 1 38.4MHZ
SLM CH1 CTL1 XO TXCO SEL
0: XO
1: TCXO
Title
K81A_TEST_BOARD
Size
A3
Document Number
PM855B Charger
Rev
P0
Date:
Monday, June 13, 2022
Sheet
24
77



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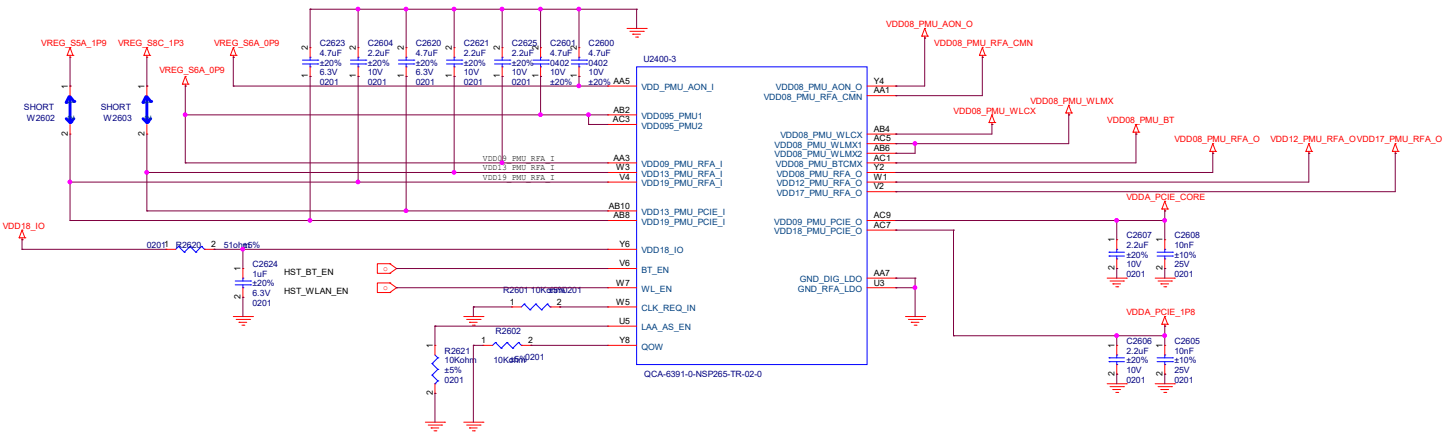
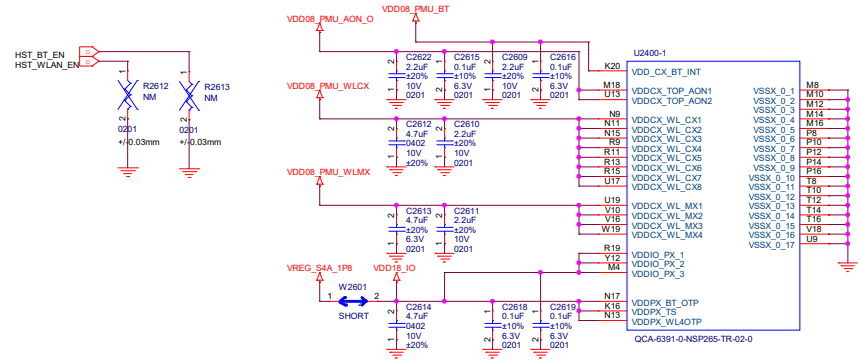
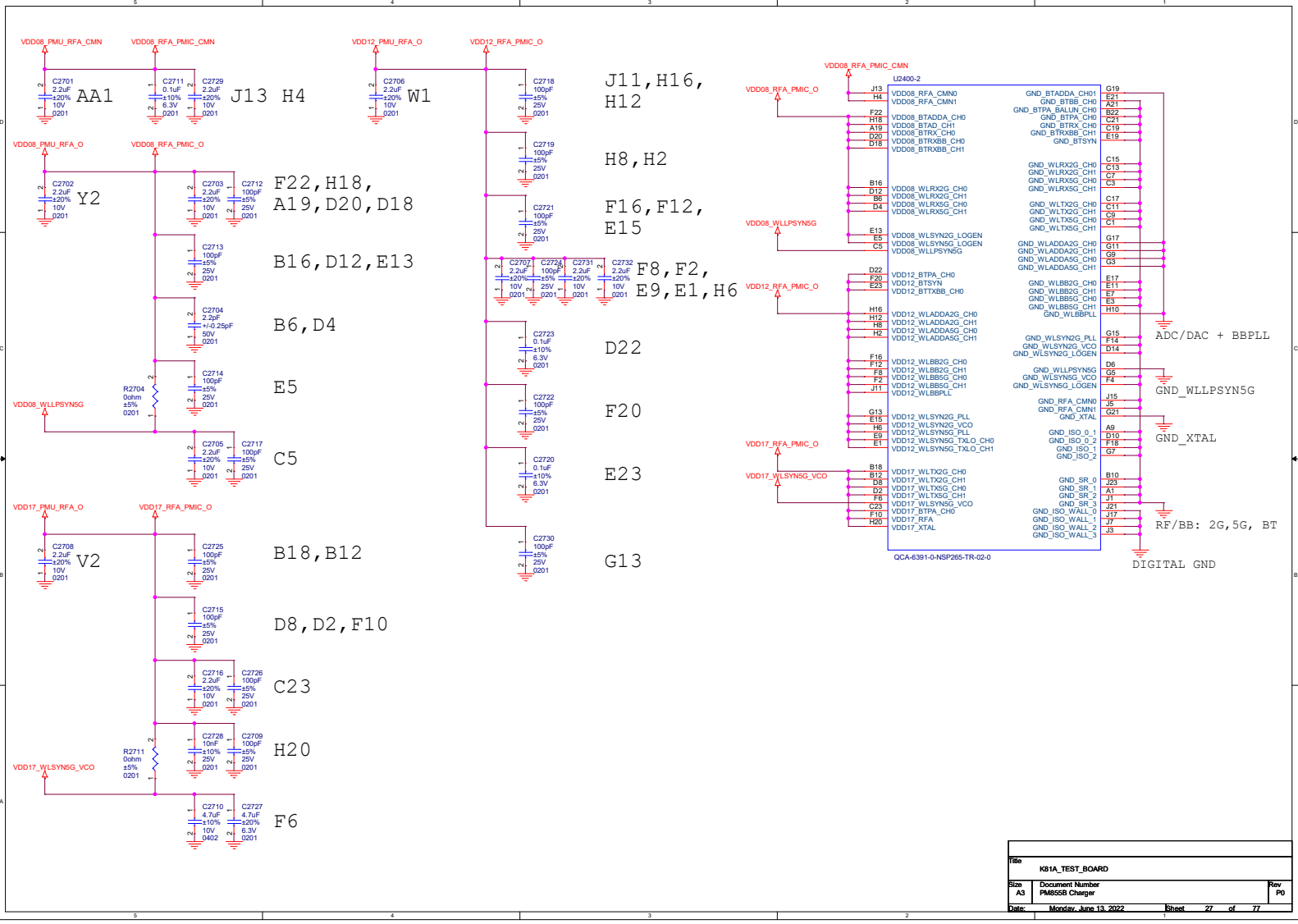
Size	
Number/Revision	
Date	Monday, June 14, 2021
Sheet	
Author	Pegatron



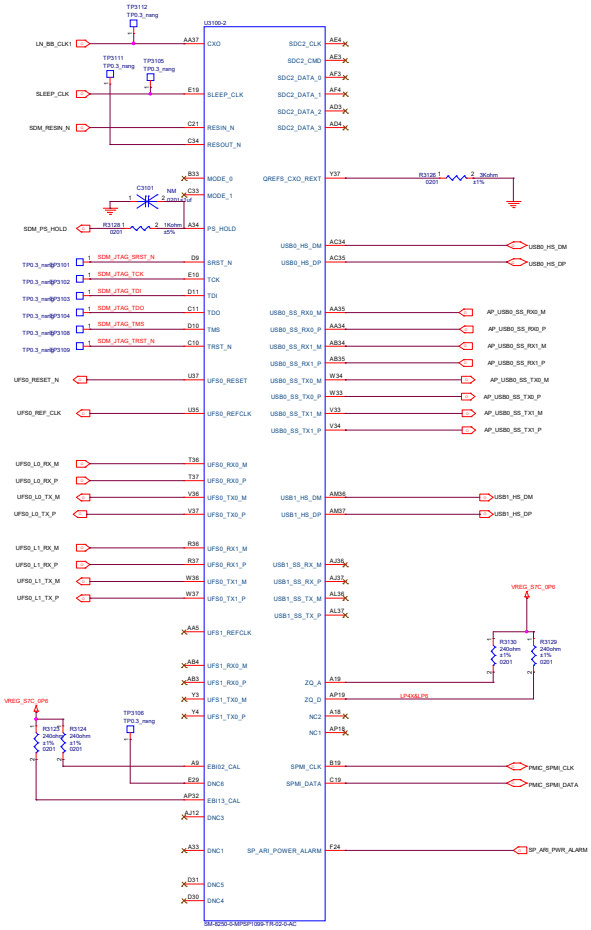


Title	K81A_TEST_BOARD	
Size A3	Document Number PM855B Charger	Rev P0
Date: Monday, June 13, 2022	Sheet	

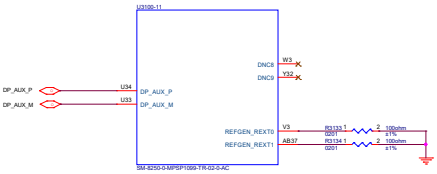


Title	K81A_TEST_BOARD		
Size A3	Document Number PM855B Charger		Rev P0
Date: Monday, June 13, 2022		Sheet 27 of 77	

We use current SM8250 symbol as LP5 PKG, and it can be compatible with LP4x PKG



LP5 DNI R3135/R3136, MOUNT R3130,R3129



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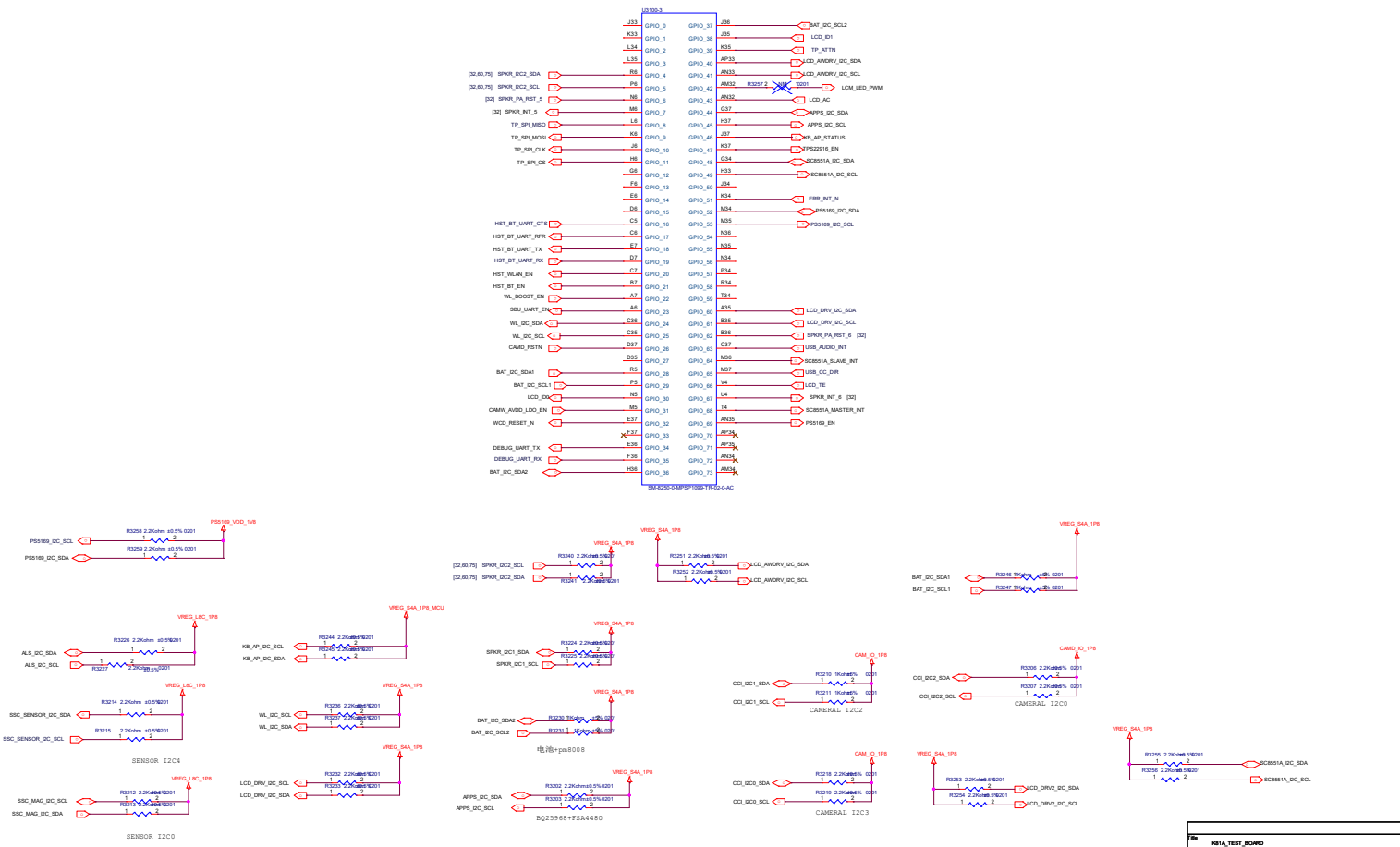
Size A2	Document Number SDM855 Control		Rev P0
Date: Monday, June 13, 2022		Sheet	



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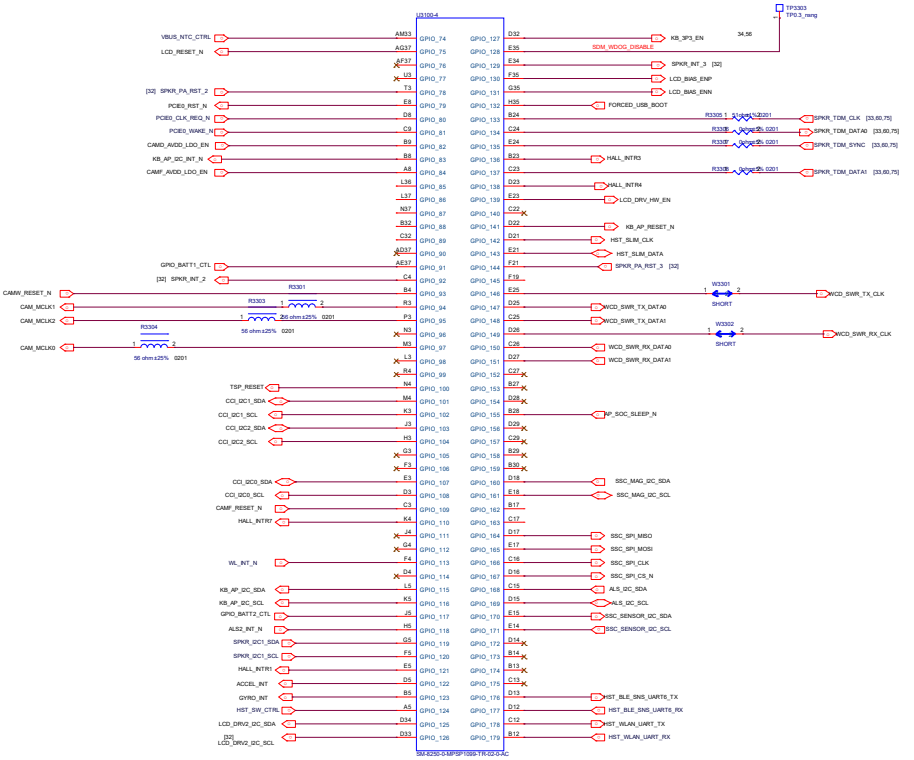
Size A2	Document Number SDM850 GPIO-1		Rev P0
Date: Monday, June 13, 2022		Sheet 33 of 77	



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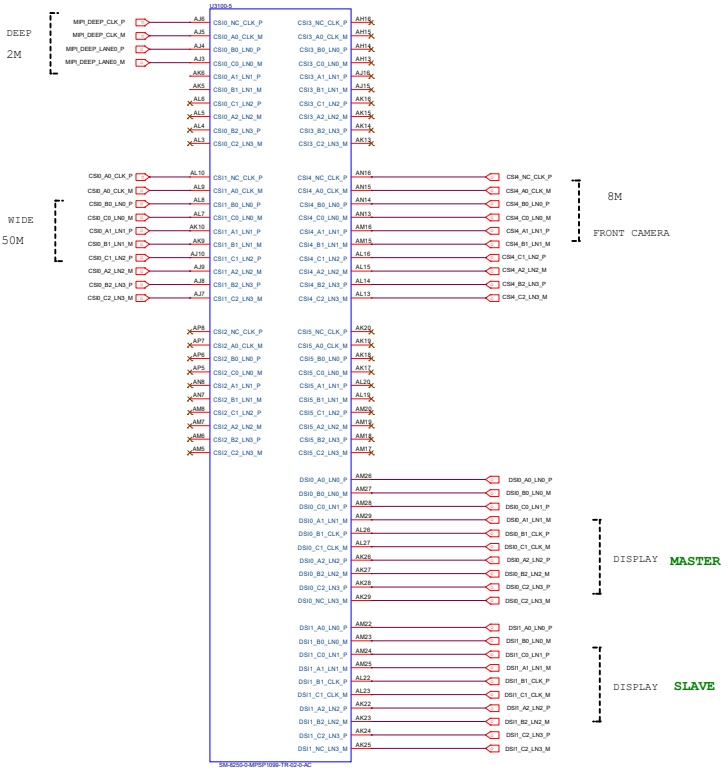
Size: A2	Document Number: SDM855 GPIO-2		Rev: P0
Date: Monday, June 13, 2022		Sheet 34 of 77	



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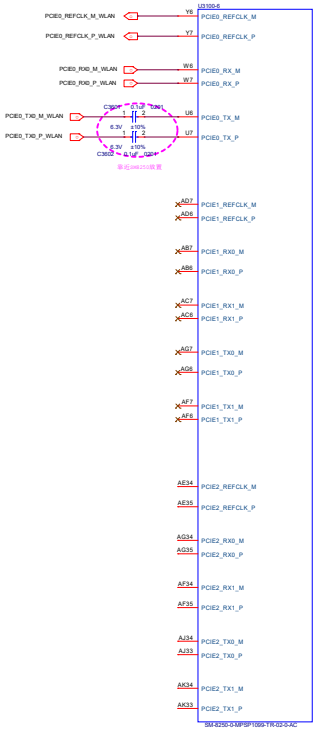
Size A2	Document Number SDM850 MIPI	Rev P0
Date: Monday, June 13, 2022	Sheet 35 of 77	



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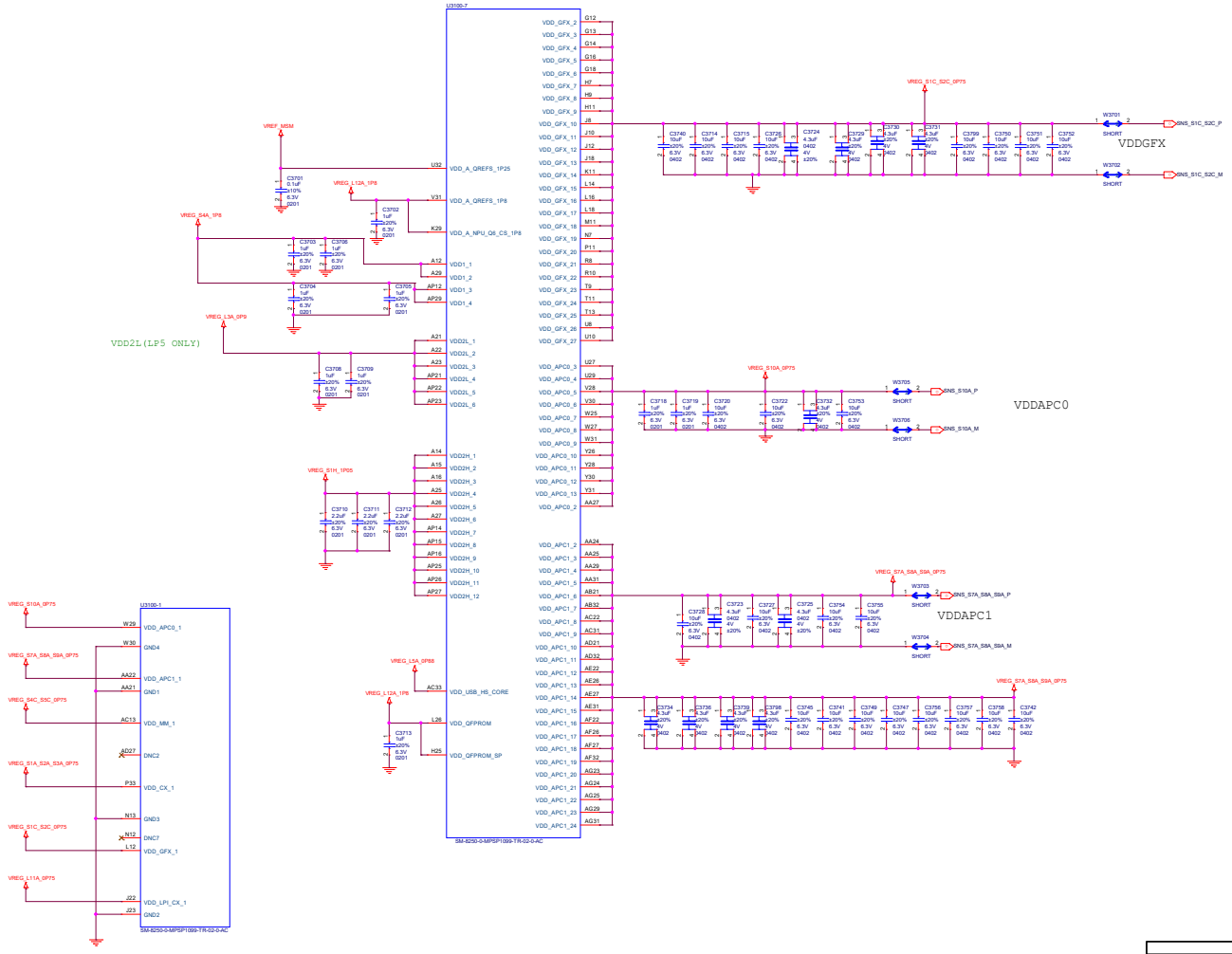
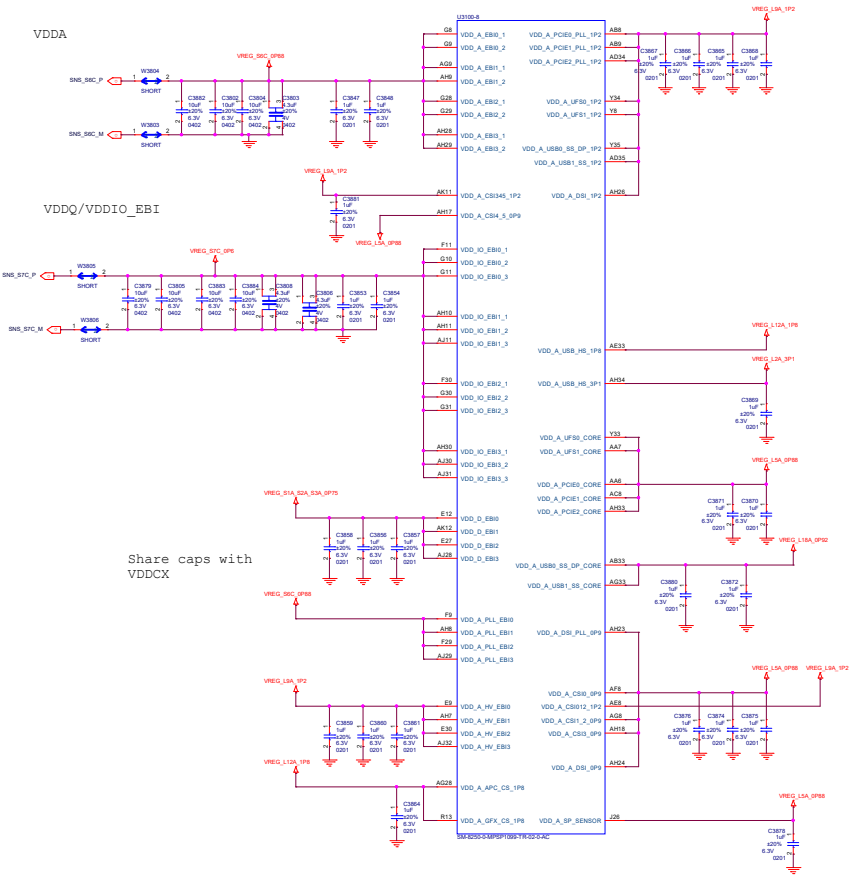
Size A2	Document Number SDM850 RF INTF	Rev P0
Date: Monday, June 13, 2022	Sheet 37 of 77	



Title	K81A_TEST_BOARD	
Size A2	Document Number SDM850-PWR1	Rev P0
Date: Monday, June 13, 2022	Sheet 38 of 77	



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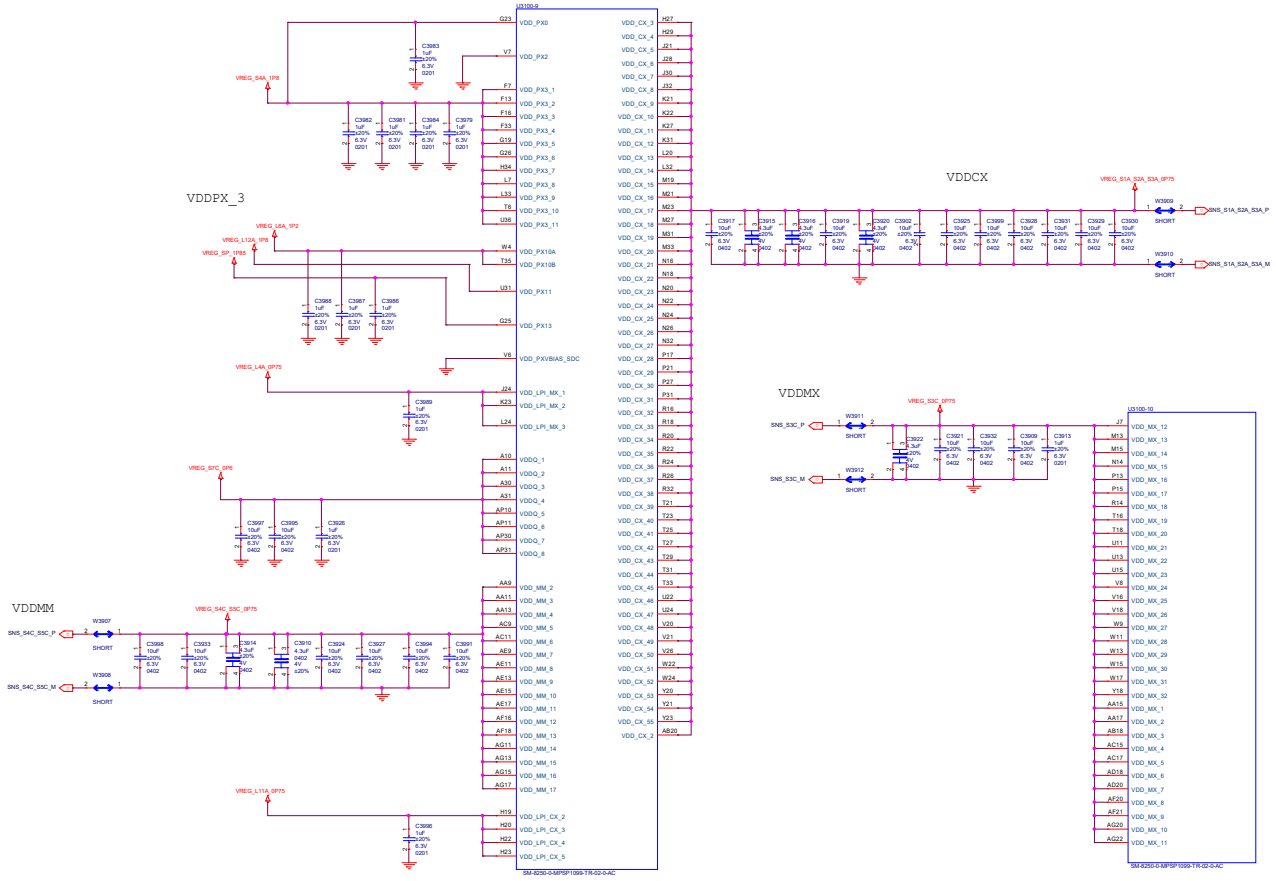
Size	Document Number		Rev
A2	SDM850-PWR2		P0
Date:	Monday, June 13, 2022	Sheet 30 of 77	



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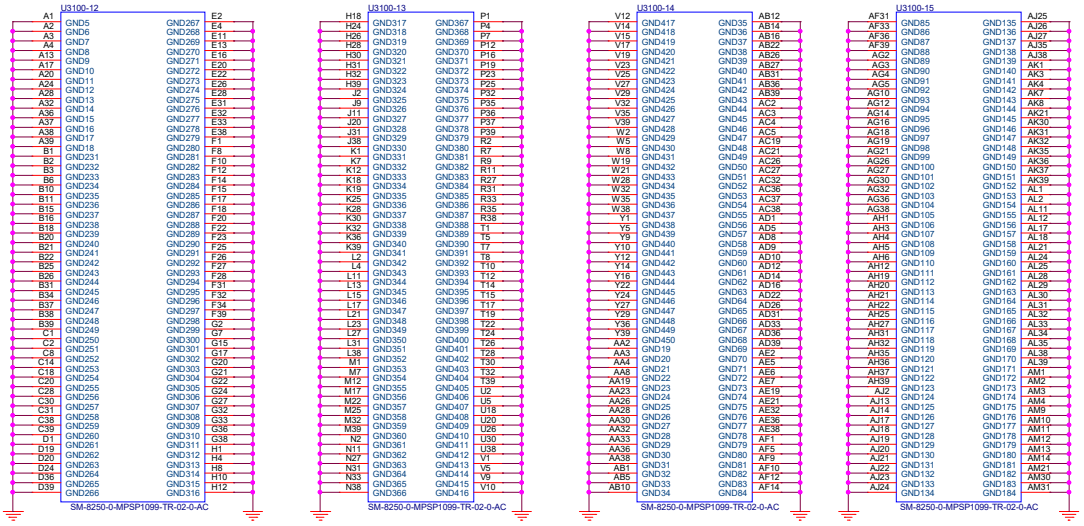
Size A2	Document Number SDM850-PWR3		Rev P0
Date: Monday, June 13, 2022		Sheet 40 of 77	



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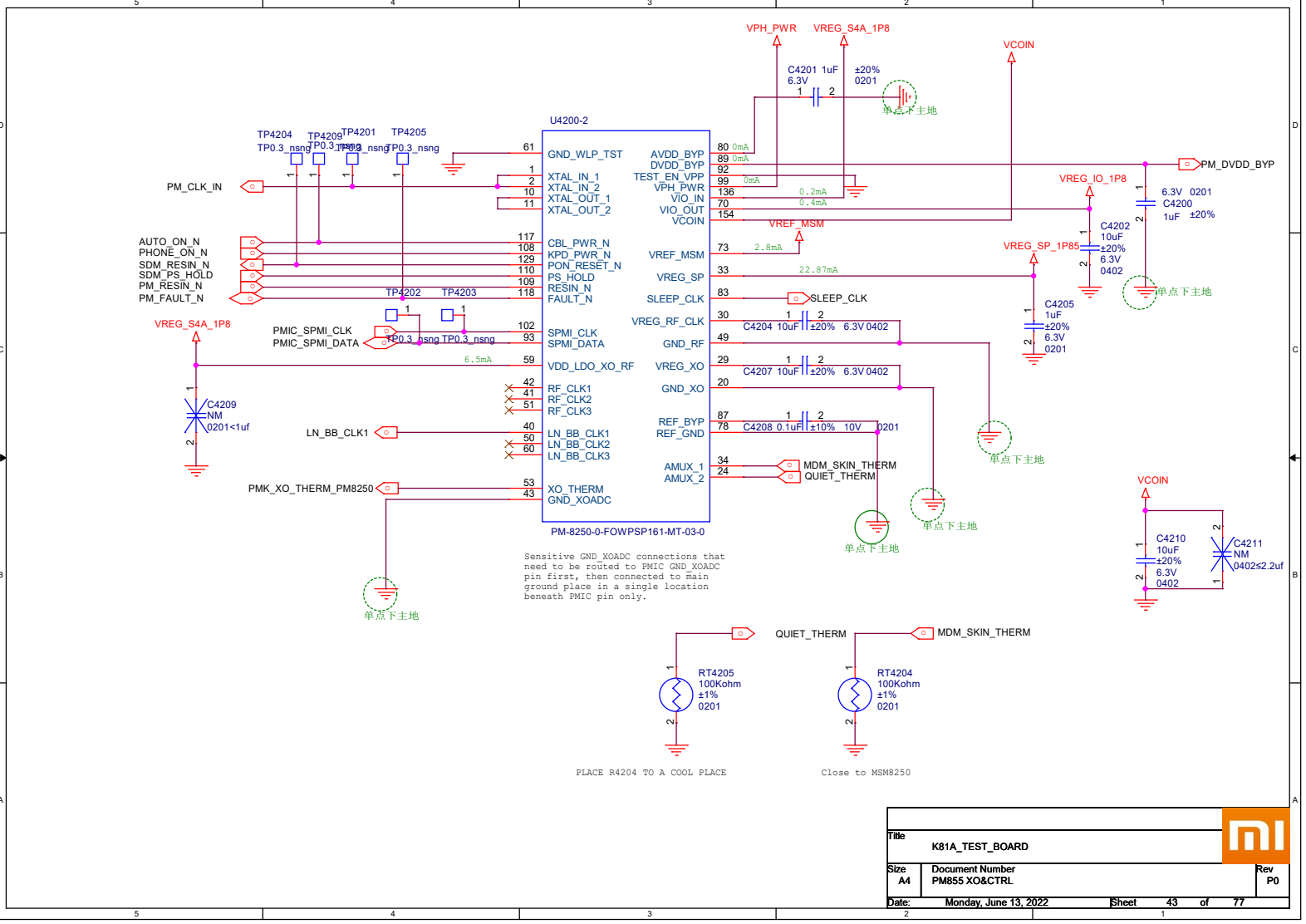
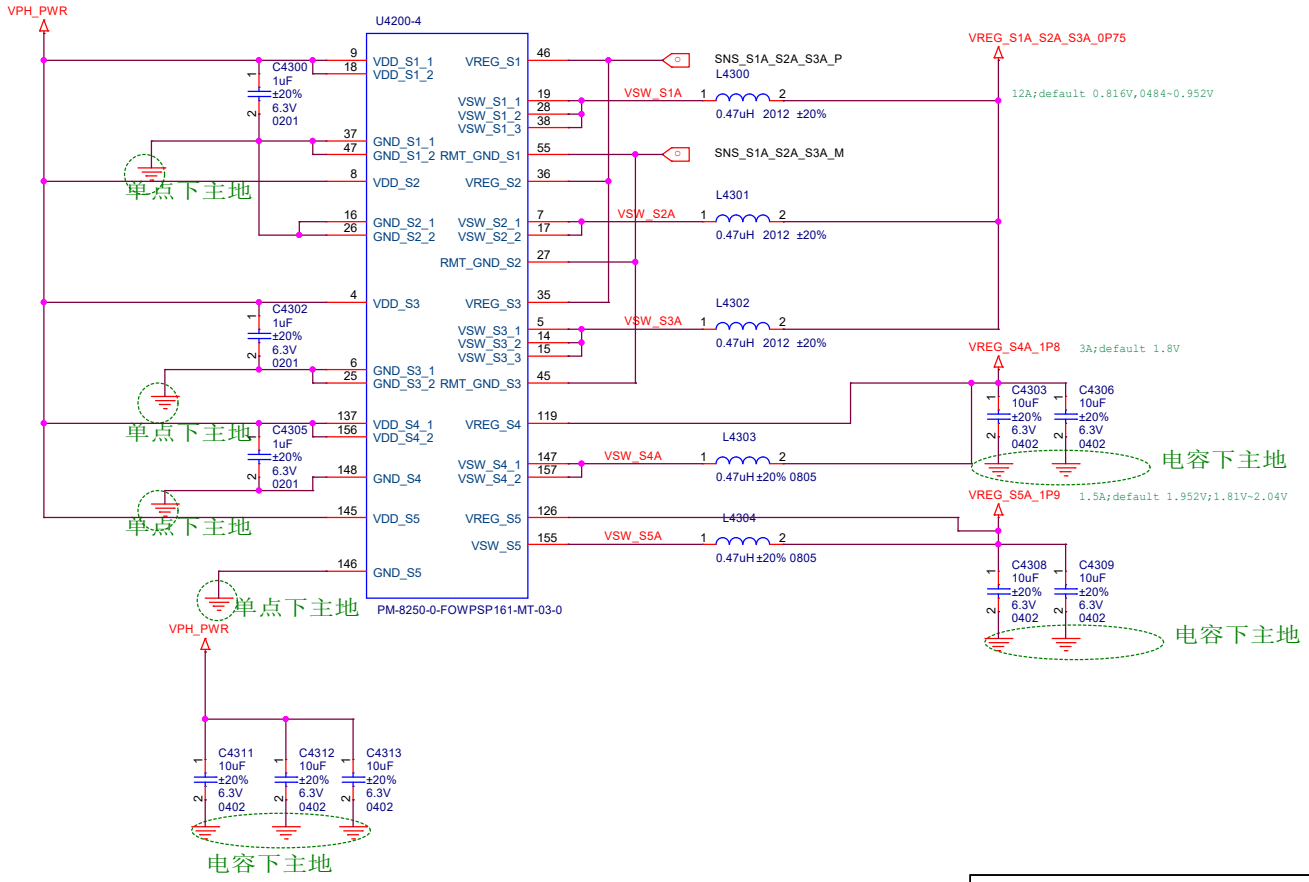
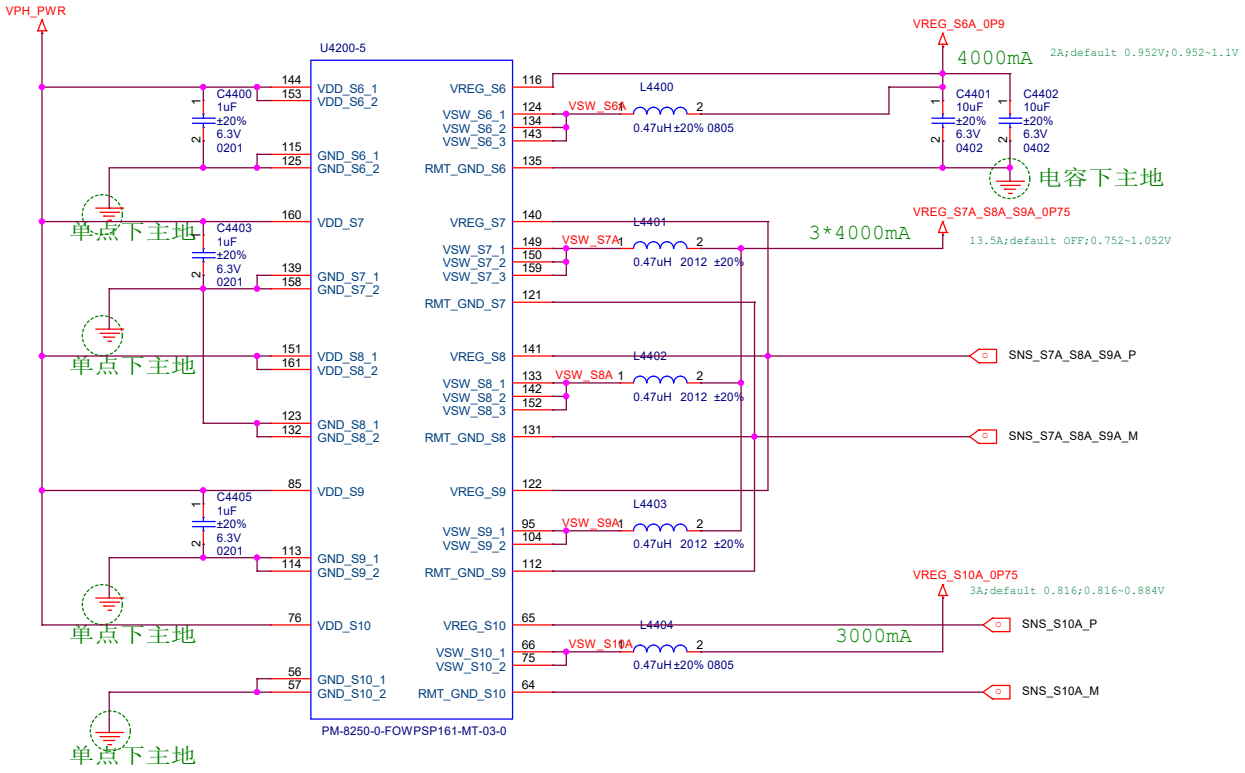
Date: Monday, June 13, 2022		Sheet 42 of 77	



Title	K81A_TEST_BOARD	
Size A4	Document Number PM855 XO&CTRL	Rev P0
Date: Monday, June 13, 2022	Sheet 43 of 77	



Title	K81A_TEST_BOARD	
Size A4	Document Number PM855 BUCK CONVERTER1	Rev P0
Date: Monday, June 13, 2022	Sheet 44 of 77	



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Size A4	Document Number PM855 BUCK CONVERTER2		Rev P0
Date: Monday, June 13, 2022	Sheet 45 of 77		

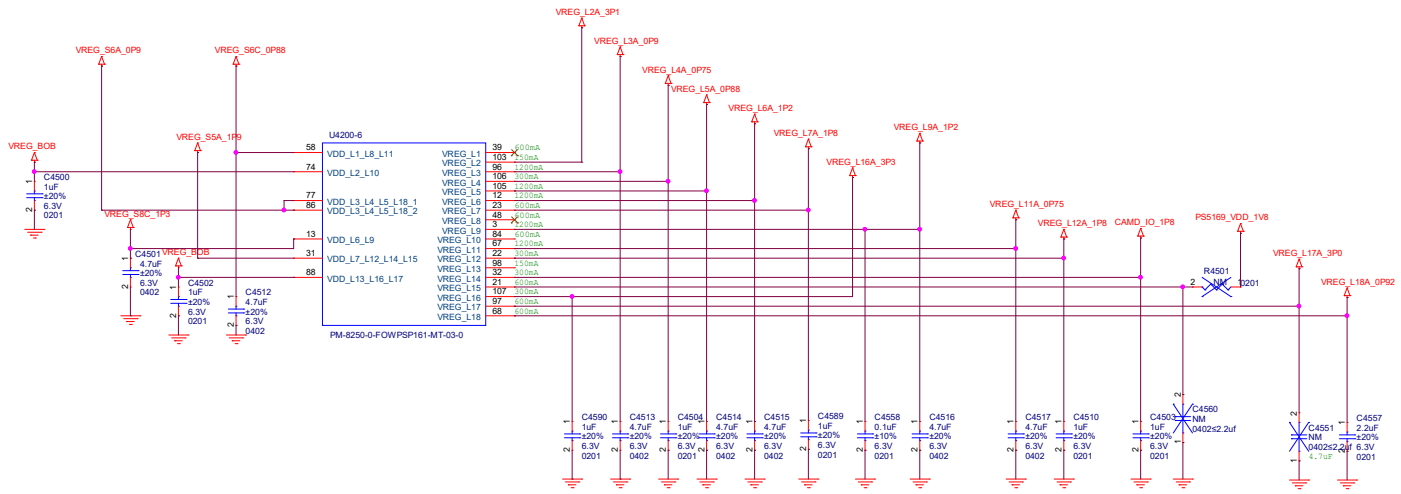


Table 3-9 PM8250 linear/low-voltage regulator summary

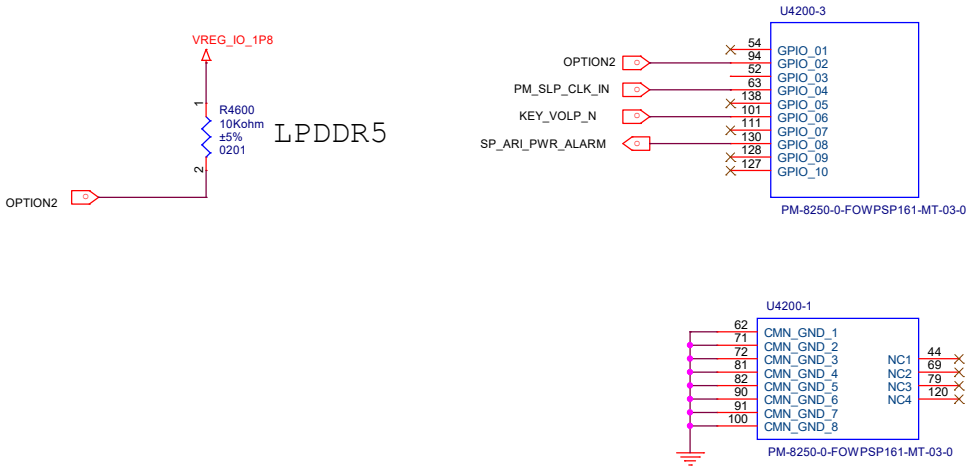
Regulator	Circuit type	I_{RATED} (mA) [1]	Default on booting voltage (V) [2]	Nominal voltage (V)	Active voltage minimum (V)	Active voltage maximum (V)	Expected use
L1A	LDO510 NMOS 600	600	–	0.752			Spare
L2A	LDO510 MV PMOS 150	150	3.072	3.072	3.072	3.072	USB
L3A	LDO510 NMOS 1200	1200	0.928	0.928			LPDDR5: VDD2L LPDDR4X: Spare
L4A	LDO510 NMOS 300	300	0.816	0.816	0.752	0.904	LPI_MX
L5A	LDO510 NMOS 1200	1200	0.88	0.88	0.88	0.88	LPI_MX
L6A	LDO510 NMOS 1200	1200	1.2	1.2	1.2	1.2	UFS VCCQ, PX_10
L7A	LDO510 LV PMOS 600	600	–	1.704			QCA6390 VDDRFA backup
L8A	LDO510 NMOS 600	600	–	0.816			Spare
L9A	LDO510 NMOS 1200	1200	1.2	1.2	1.2	1.2	1.2V VDDA for DSI, PCIE, HV EBI, USB_SS_DP_1P2, CSI, and so on.

Table 3-9 PM8250 linear/low-voltage regulator summary (cont.)

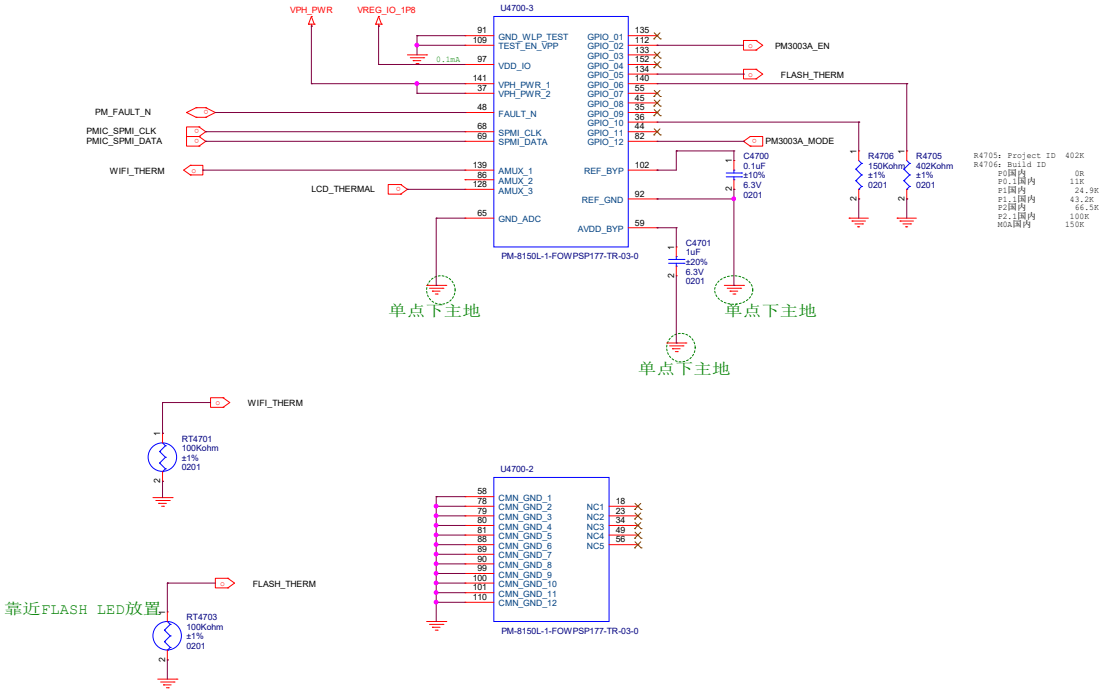
Regulator	Circuit type	I_{RATED} (mA) [1]	Default on booting voltage (V) [2]	Nominal voltage (V)	Active voltage minimum (V)	Active voltage maximum (V)	Expected use
L10A	LDO510 MV PMOS 600	600	–	2.904			Optional DMIC Bias
L11A	LDO510 NMOS 1200	1200	0.816	0.816			LPI_CX
L12A	LDO510 LV P300	300	1.8	1.8	1.8	1.8	BBCLK, USB, UFS, QFPROM
L13A	LDO510 MV P150	150	–	3.008			FTM TSP_AVDD
L14A	LDO510 LV P300	300	–	1.8	1.8	1.8	OLED_VDDIO
L15A	LDO510 LV P600	600	–	1.704	1.704	1.704	QCA6436 VCC_1P8
L16A	LDO510 MV P300	300	–	3.024			Ext BT xPA 3p3
L17A	LDO510 MV P600	600 [3]	2.96	2.96	2.856	3.008	UFS_2L_VCC
L18A	LDO510 N600	600	0.912	0.912			USB SS core & DP core

1. Some regulators are tested and used beyond their lrated limit
2. Voltages shown in the *Default on booting voltage (V)* column indicate that the regulator is enabled as part of the hardware default-on sequence.
3. VREG_L17A has been specifically validated up to 800 mA for UFS VSS support.

Title	K81A_TEST_BOARD	
Size A3	Document Number PM8655 LDOs	Rev P0
Date: Monday, June 13, 2022	Sheet 46 of 77	



Title	K81A_TEST_BOARD	
Size A4	Document Number PM855 GPIO&GND	Rev P0
Date: Monday, June 13, 2022	Sheet 47 of 77	



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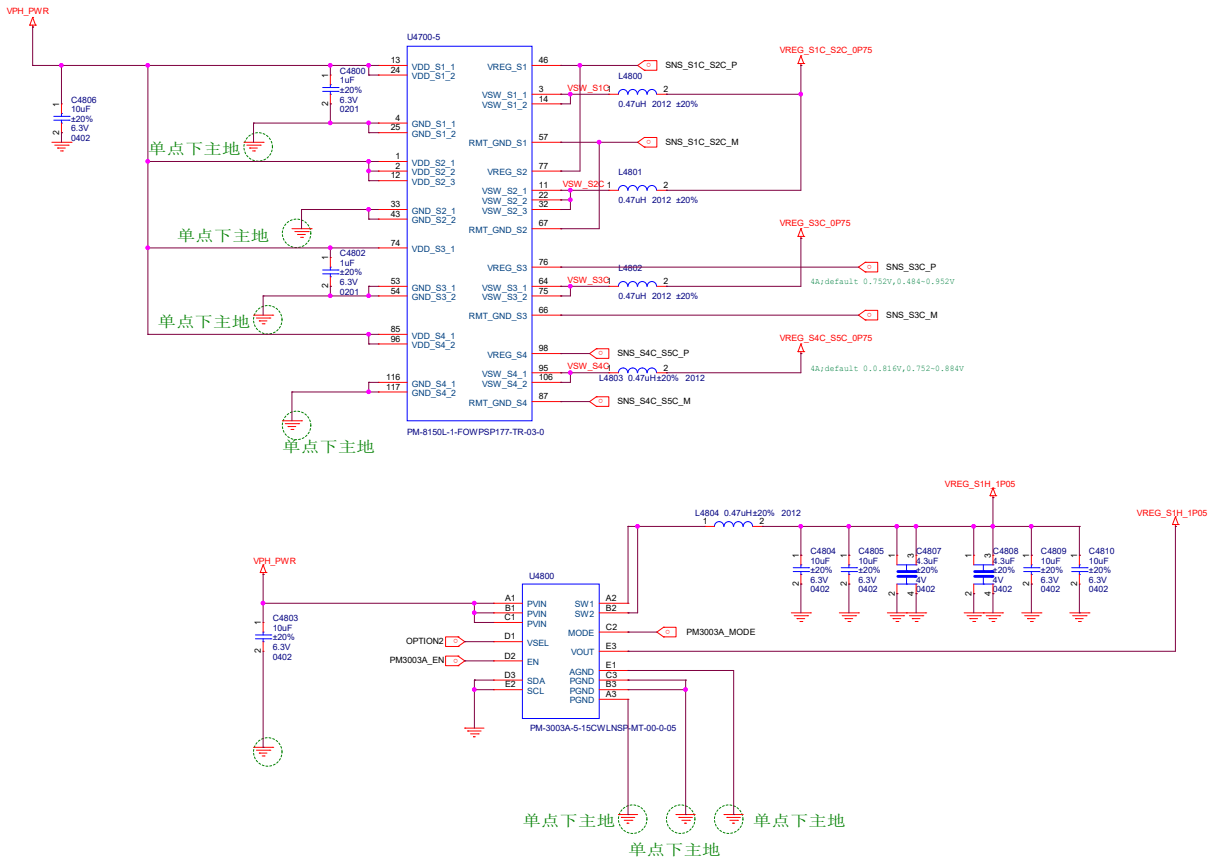
Size A3	Document Number PM855A CTRL&GND	Rev P0
Date: Monday, June 13, 2022	Sheet 48 of 77	



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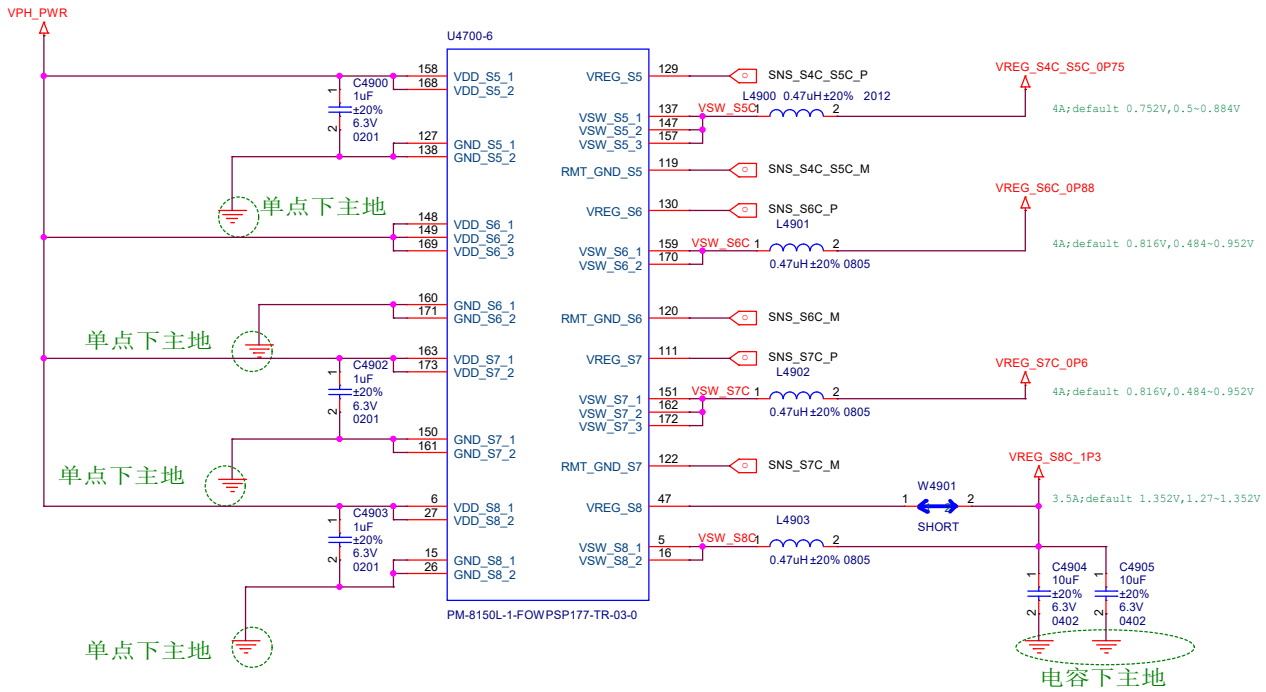
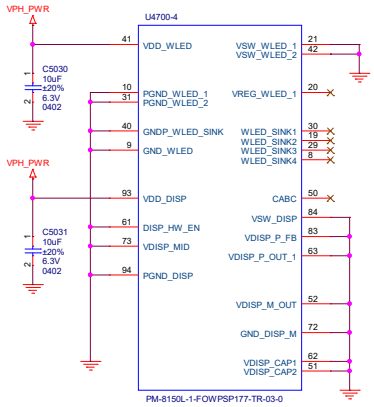
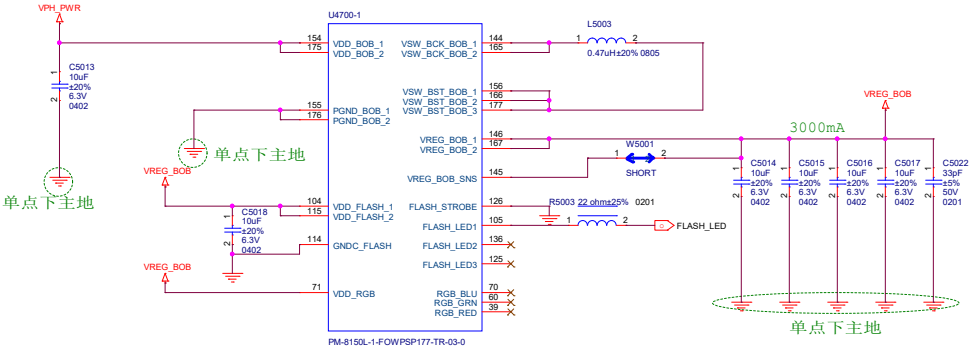
Size A3	Document Number PM655A BUCK CONVERTER1		Rev P0
Date: Monday, June 13, 2022	Sheet 49 of 77		

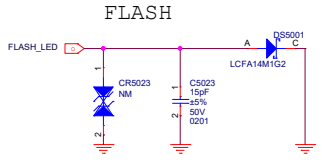


Title	K81A_TEST_BOARD	
Size A4	Document Number PM655A BUCK CONVERTER2	Rev P0
Date: Monday, June 13, 2022	Sheet 49 of 77	

Make sure SCP(short circuit peotection) must be disabled







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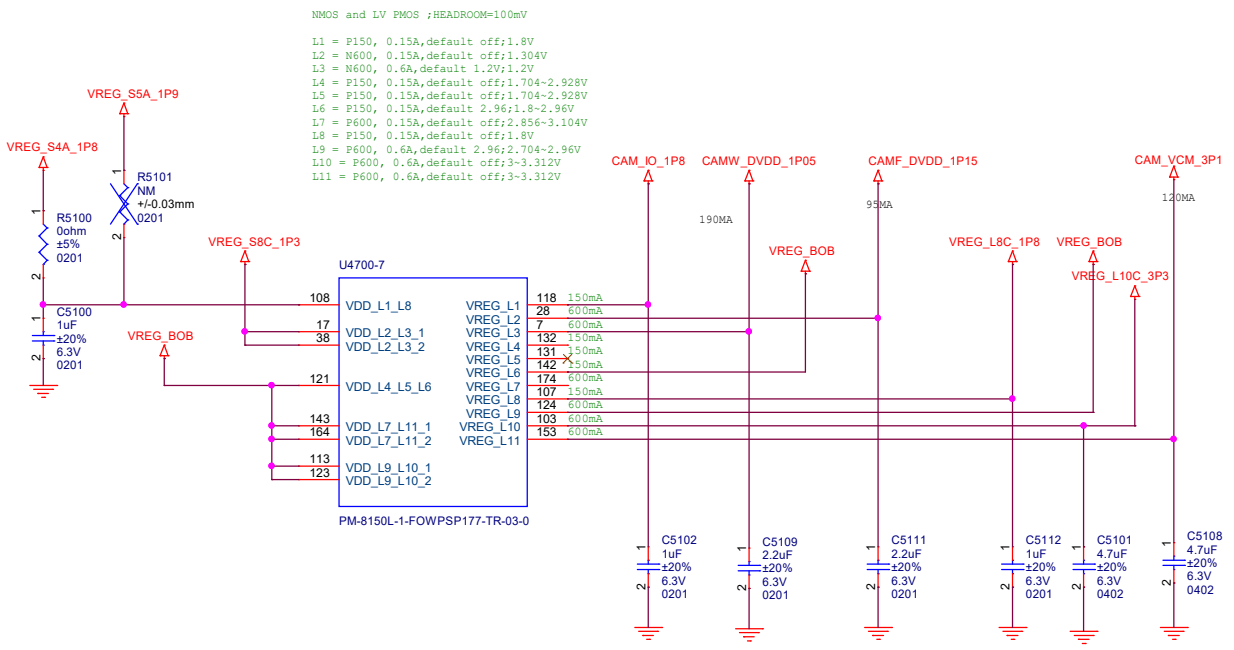
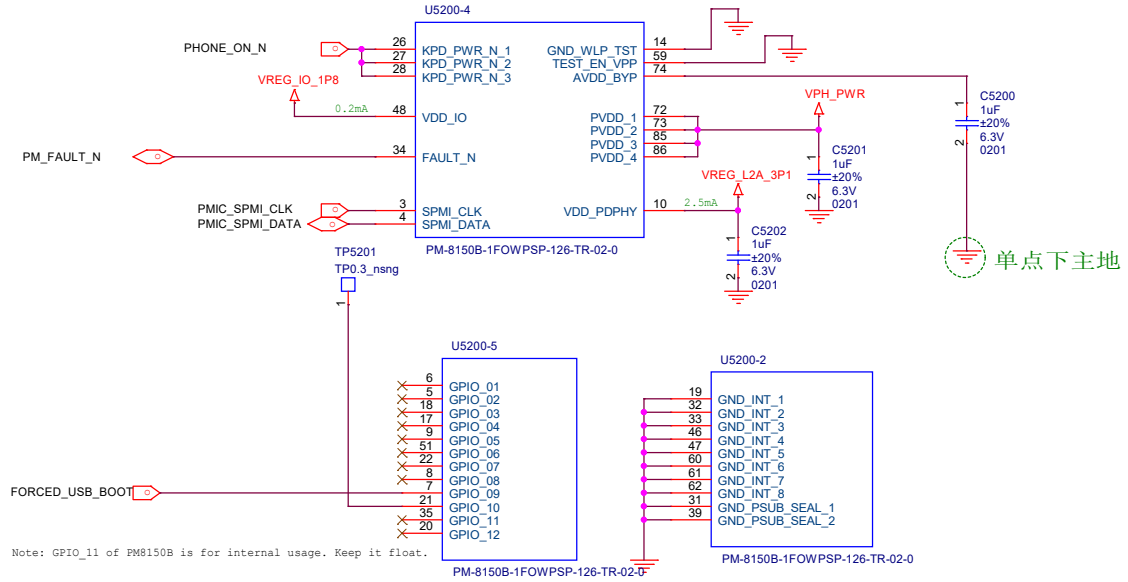
Size A3	Document Number PM855A AMOLED&BOB&FLASH	Rev P0
Date: Monday, June 13, 2022	Sheet 50 of 77	



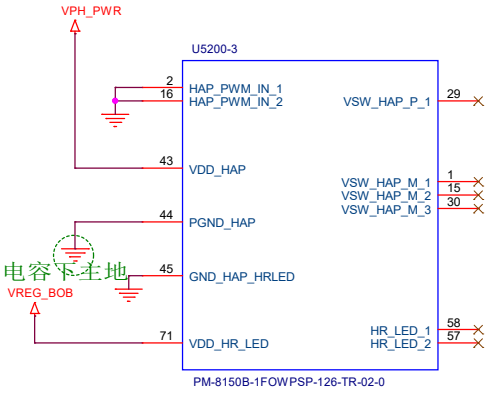
Title	K81A_TEST_BOARD	
Size A4	Document Number PM8655A LDOs	Rev P0
Date: Monday, June 13, 2022	Sheet 51 of 77	



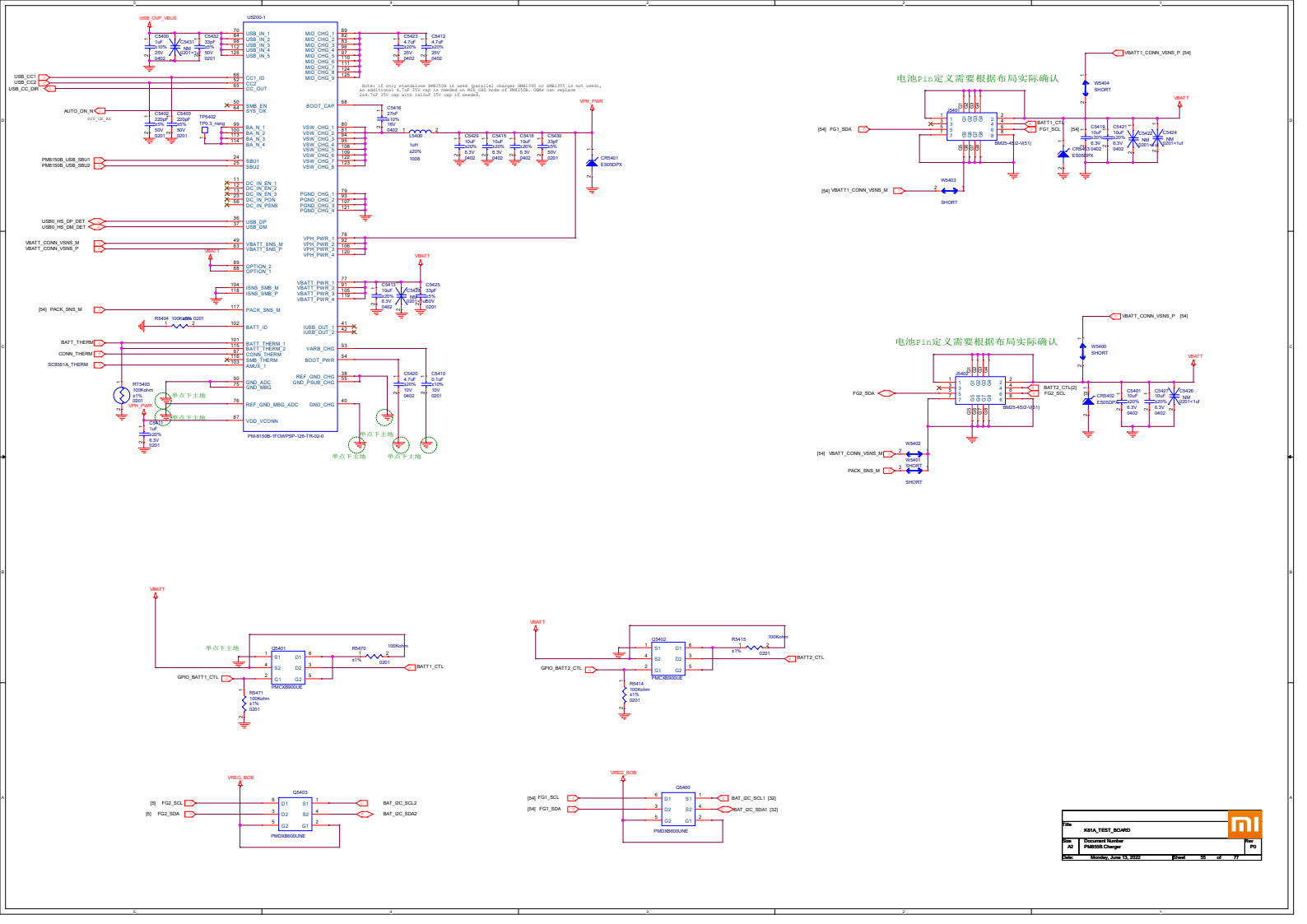
Note: GPIO_11 of PM8150B is for internal usage. Keep it float.

Note: GPIO_04 and GPIO_11 of PM8150B are for internal usage. Keep them float.
Keep GPIO_03 of PM8150B float. Don't use it for other purpose.
GPIO_06 of PM8150B is dedicated for SMB_STAT. Don't use it for other purpose.

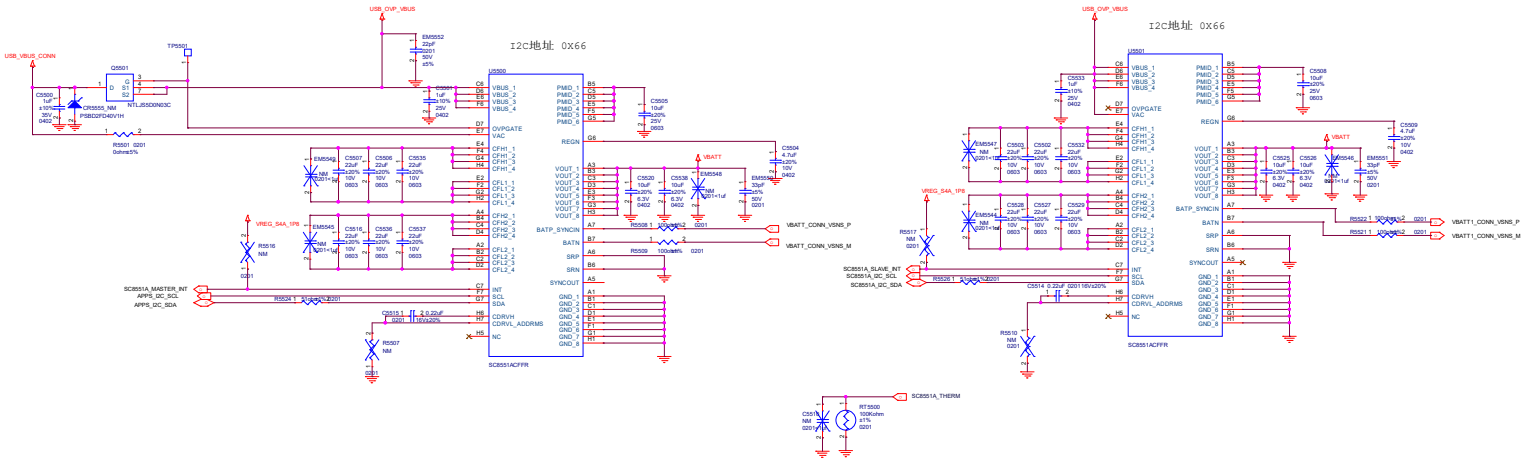
Title	K81A_TEST_BOARD	
Size A4	Document Number PM8550B CTRL&GND	Rev P0
Date: Monday, June 13, 2022	Sheet 53 of 77	



Title	K81A_TEST_BOARD	
Size A4	Document Number PM8550B HAPTIC	Rev P0
Date: Monday, June 13, 2022	Sheet 54 of 77	

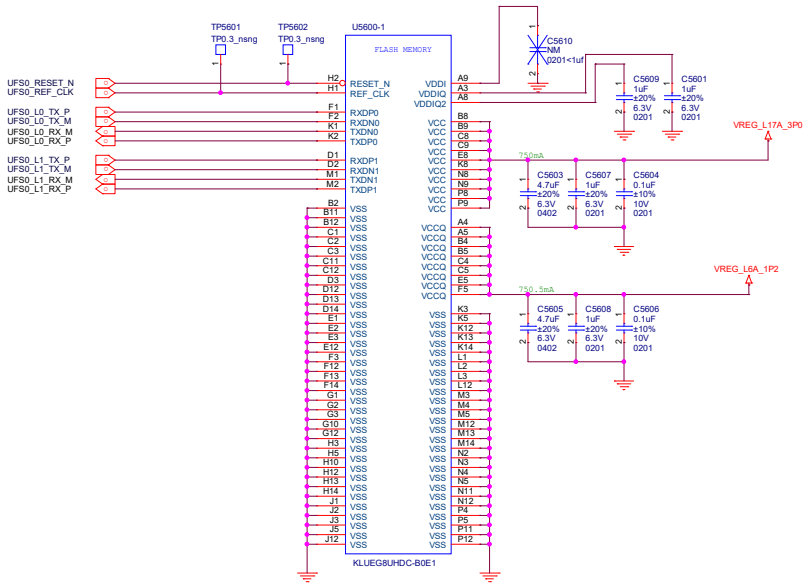


Title	K91A_TEST_BOARD
Size: A2	Document Number: PM8550 Charger
Rev: P0	
Date: Monday, June 13, 2022	Sheet 55 of 77



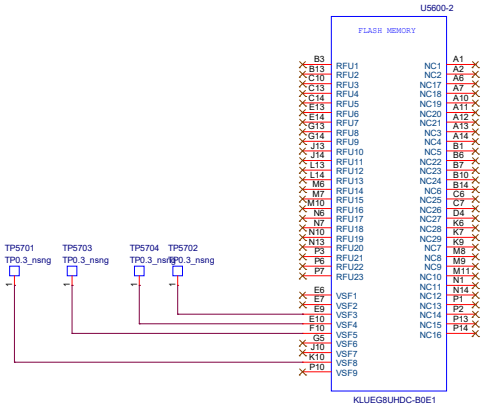
两个SC8551A工作在Standlone模式

Title	K81A_TEST_BOARD		
Size A2	Document Number SM8133B6		Rev P0
Date: Monday, June 13, 2022		Sheet 50 of 77	

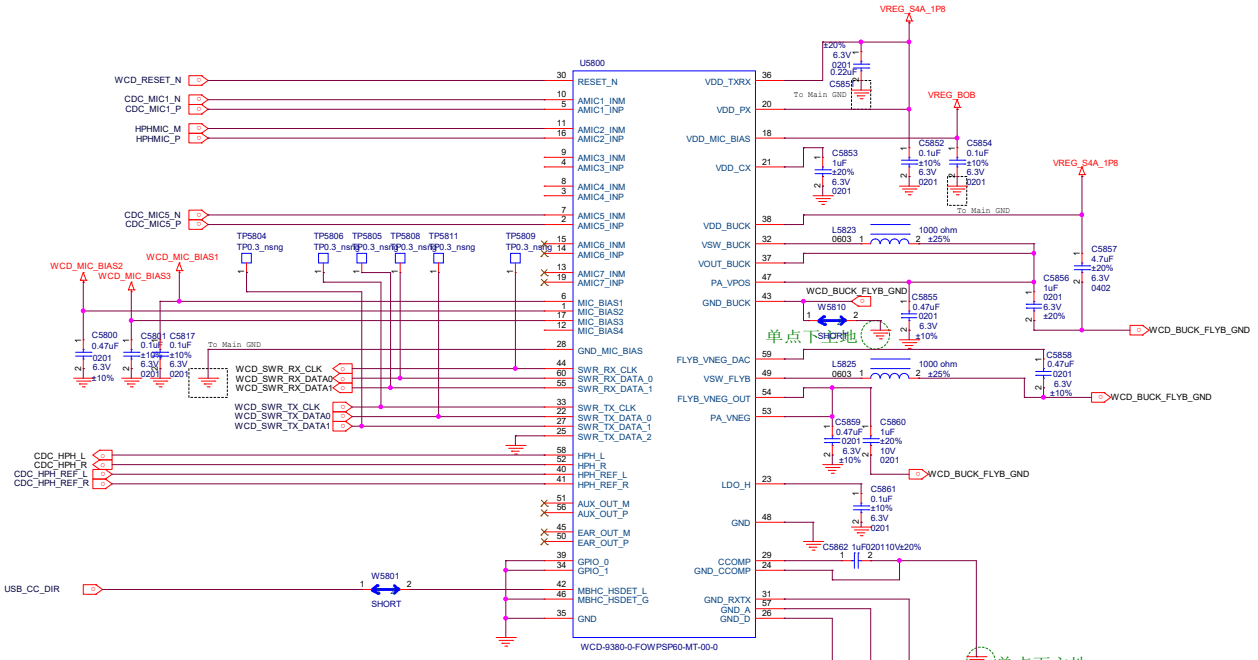


项目	配置	小米料号	P/N	供应商	描述	一供/二供	制程
K81(870)	6+128 8+256	276300000B79	KLUDG4UHDC-B0E1	Samsung	128GB UFS 3.1	First Source	V6
		276300000UJY	THGJFCT0T44BAKL	Kioxia	128GB UFS 3.0	Second Source	96L
		276300000C79	KLUEG8UHDC-B0E1	Samsung	256GB UFS 3.1	First Source	V6
		276100000H52	MT62F768M64D4BG-031 WT:A	Micron	6GB LPDDR5 for 865	First Source	1ynm
		276100000J79	K3LK7K70BM-BGCP	Samsung	8GB LPDDR5 for 875	First Source	1znm
		276100000P52	MT62F1G64D8CH-031 WT:B	Micron	8GB LPDDR5 for 875	Second Source	1znm

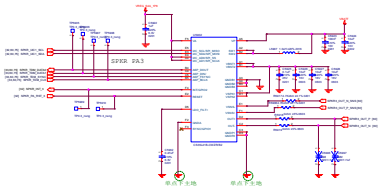
Title	K81A_TEST_BOARD	
Size A3	Document Number MEMORY	Rev P0
Date: Monday, June 13, 2022	Sheet 56 of 77	

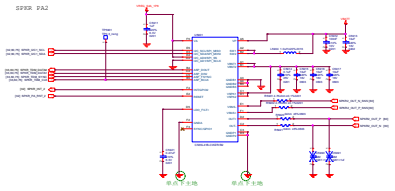


Title	K81A_TEST_BOARD		
Size A3	Document Number MEMORY-2		Rev P0
Date: Monday, June 13, 2022		Sheet 57 of 77	

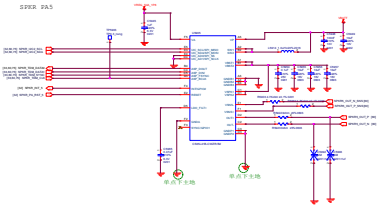


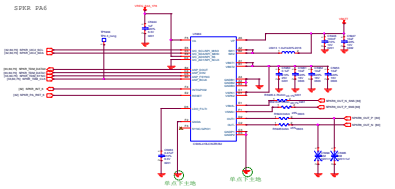
Title	K81A_TEST_BOARD		
Size A3	Document Number WCD9340-1		Rev P0
Date: Monday, June 13, 2022		Sheet 58 of 77	



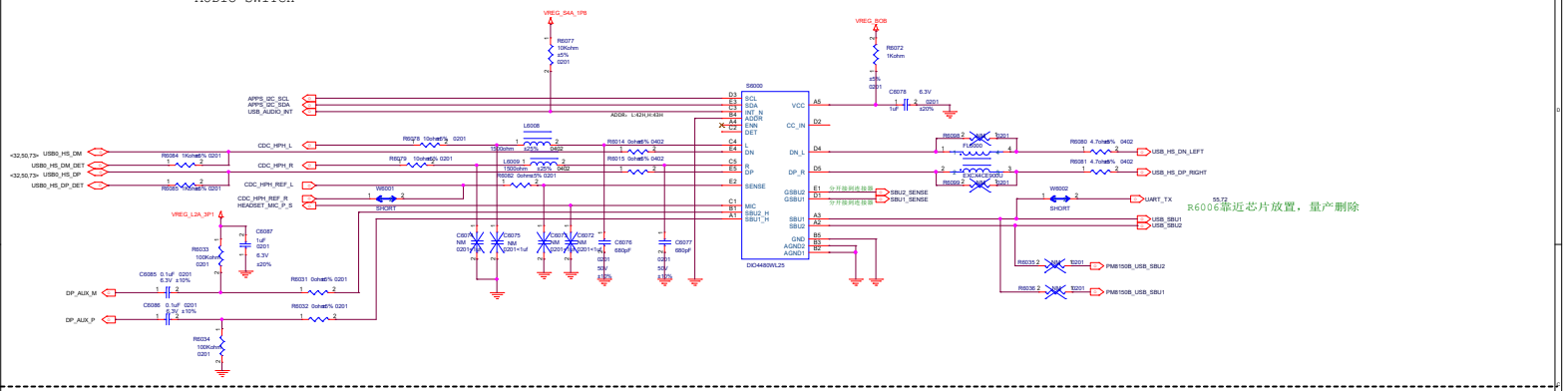


CIC_A11	CIC_A10	CIC_MOTO	CIC_MOTI	SPK
GND	GND	0x01	0x01	EPK2
TS	TS	0x03	0x01	EPK1
GND	GND	0x01	0x01	EPK3
GND	GND	0x02	0x01	EPK4

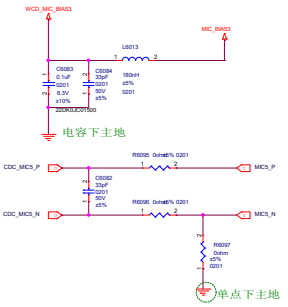




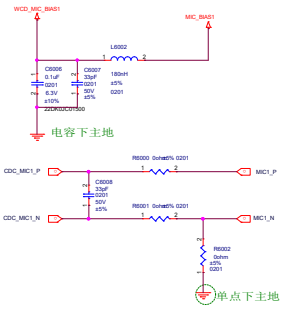
AUDIO SWITCH



TOP MIC

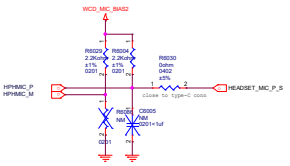


MAIN MIC



R6029、R6004、C6005靠近WCD9385（U5800）端放置

HEADSET



Title	K81A_TEST_BOARD		
Size A2	Document Number Reserved(for AUDIO)		Rev P0
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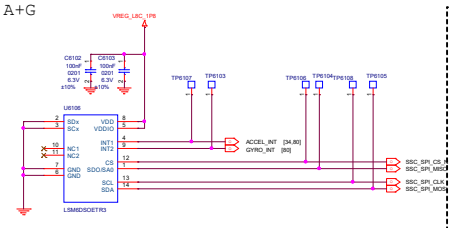
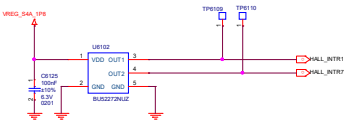
A+G

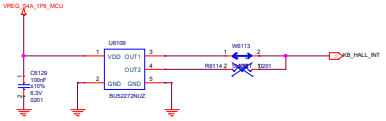


HALL

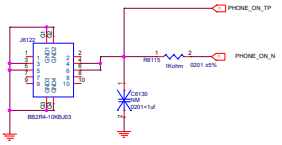
开合检测HALL



键盘在位检测HALL

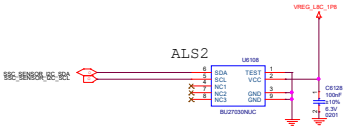


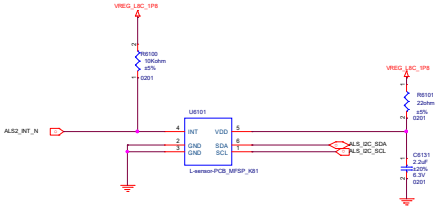
POWERKEY



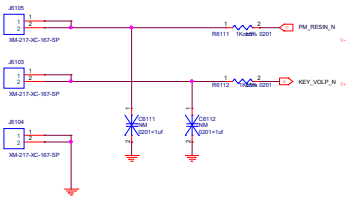
L-sensor

ALS2

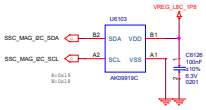


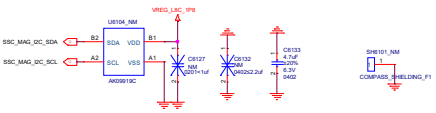


Sidekey

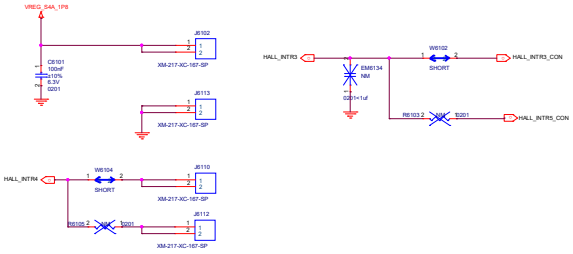


COMPASS





HALL of PAN



Title	K81A_TEST_BOARD	
Size A2	Document Number SENSOR-1	Rev P0
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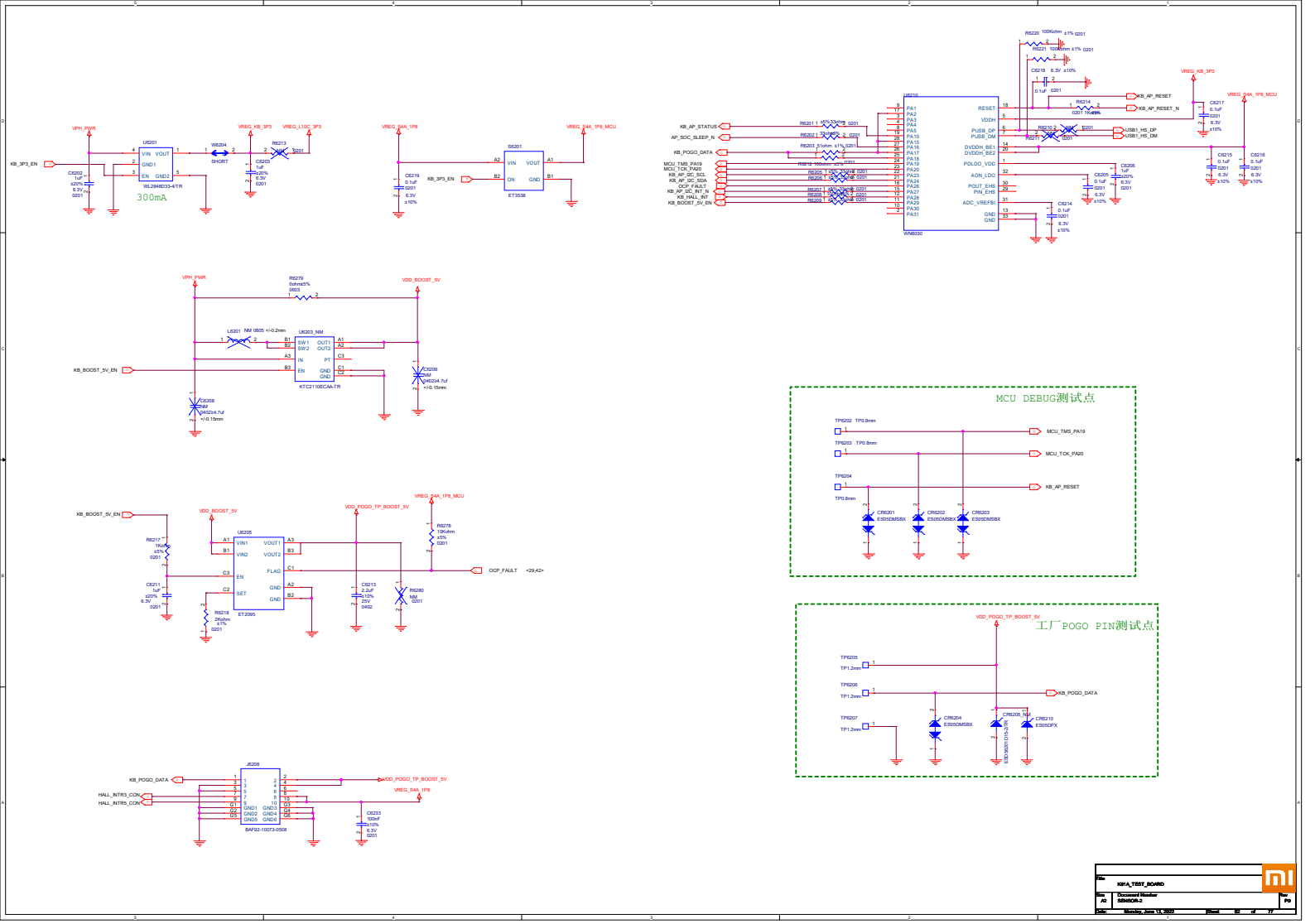
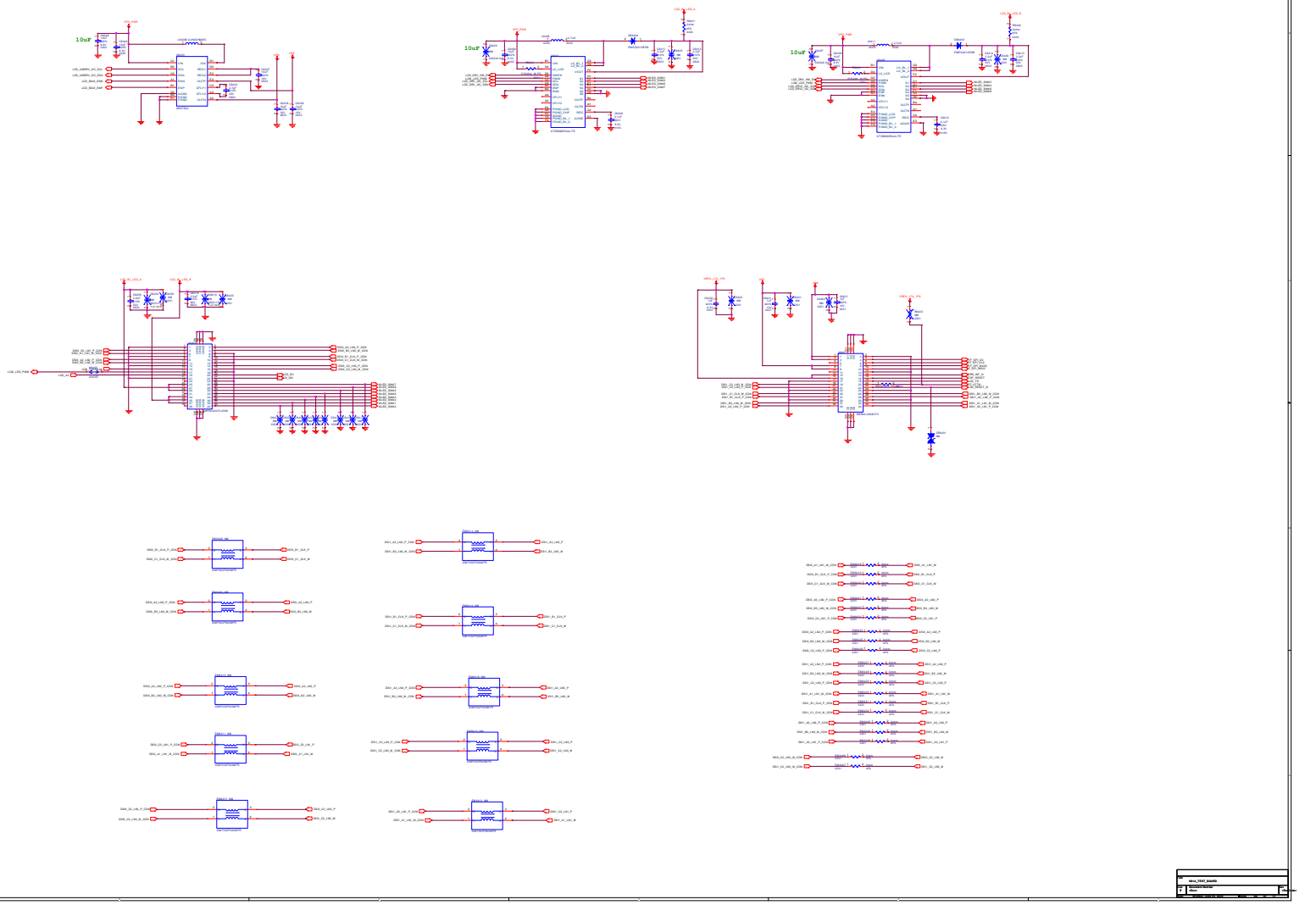
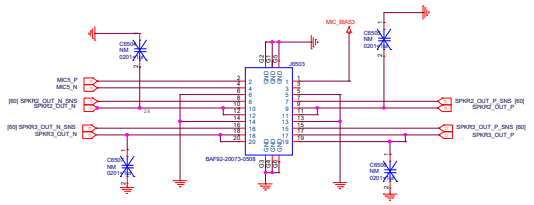
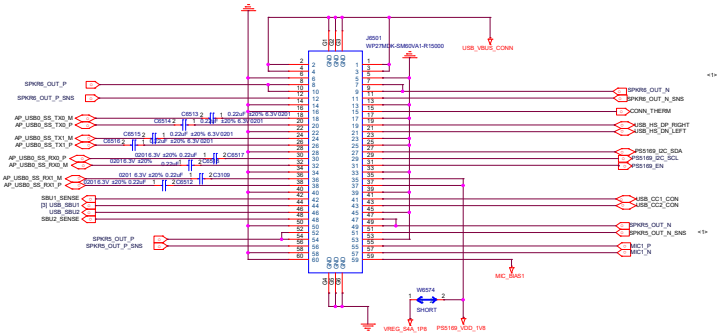


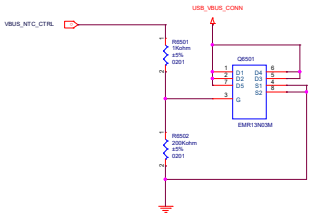
Title: K91A_TEST_BOARD		
Size: A2	Document Number: SBMOK-2	Rev: P0
Date: Monday, June 13, 2022	Sheet 62 of 77	



Date:	2014_7292_B2a0b
Sheet:	Sheet1

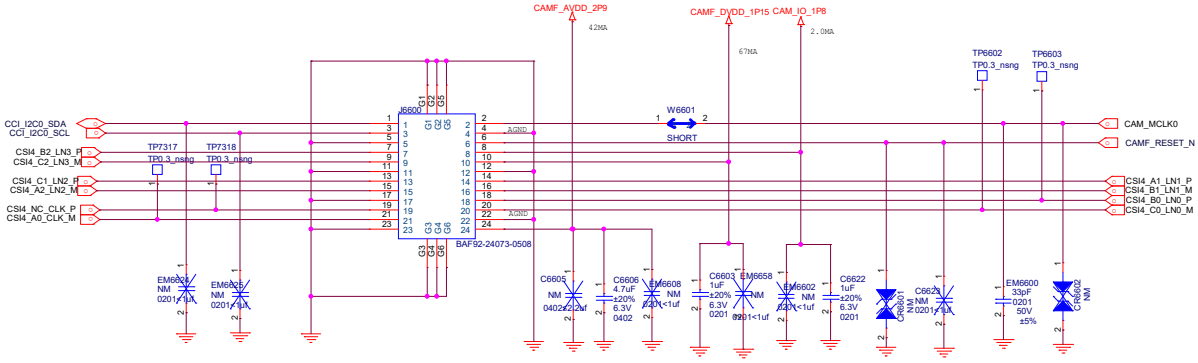






Title	K81A_TEST_BOARD		
Size A2	Document Number STB		Rev P0
Date: Monday, June 13, 2022		Sheet 65 of 77	

Front 8M (Hi846W)



Title	K81A_TEST_BOARD	
Size A3	Document Number FRONT CAMERA	Rev P0
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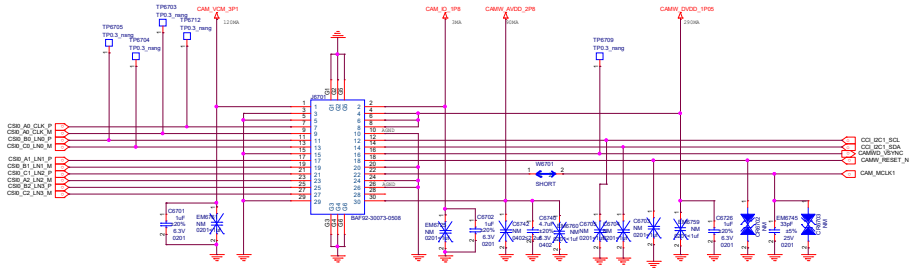
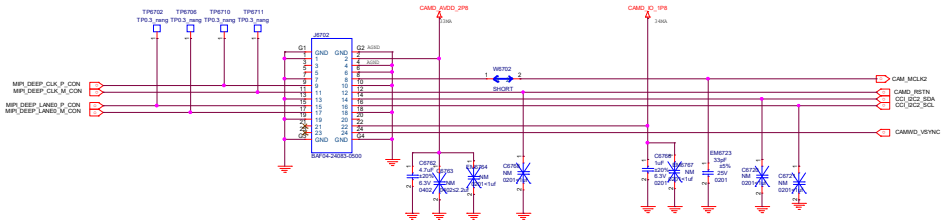
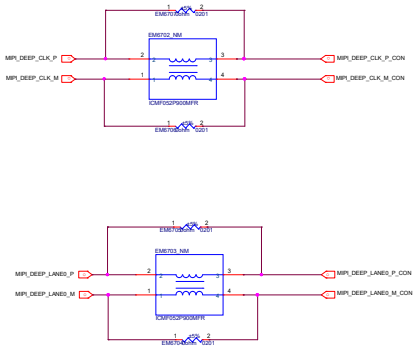
WIDE 50M(S5KJN1)



2M DEEP (OV02B1B10)





File	K81A_TEST_BOARD	
Size A2	Document Number WIDE&TELE CAMERA	Rev P0
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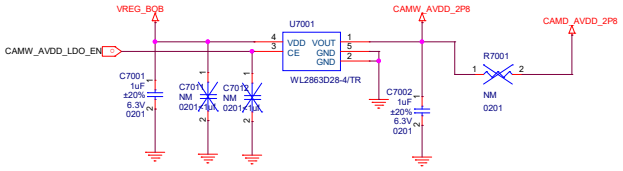
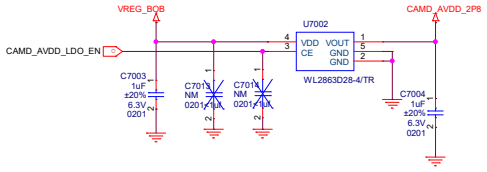
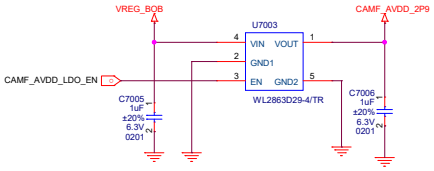
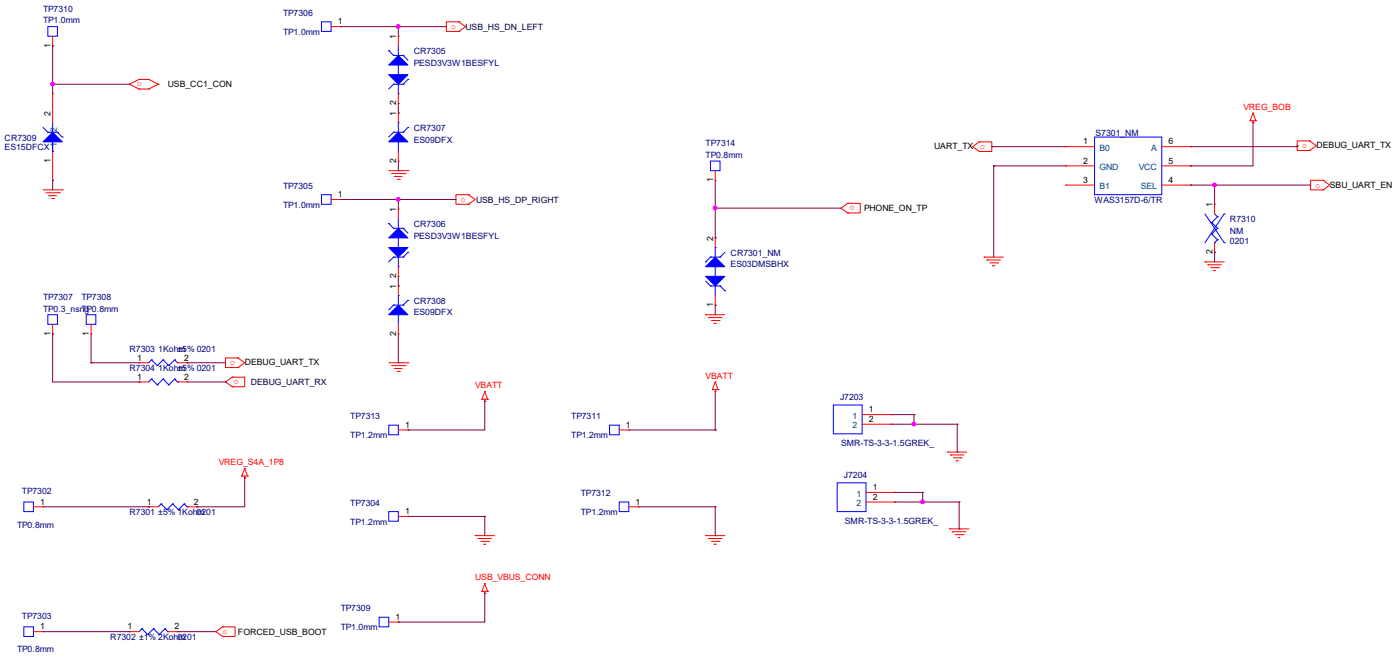






后摄deep AVDD保留外置LDO兼容设计

Title	K81A_TEST_BOARD	
Size A3	Document Number TEST POINT	Rev P0
Date: Monday, June 13, 2022	Sheet 70	77



SMT硅胶

屏蔽罩

Title	K81A_TEST_BOARD	
Size A3	Document Number PM6009	Rev P0
Date: Monday, June 13, 2022	Sheet 73 of 77	